SDHCAL for ILD

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IPNLyon

OUTLINE

- SDHCAL for ILD
- SDHCAL-GRPC prototype
- Prototype results
- Preparation for ILD
- Present and future development
- Conclusion

SDHCAL Milestones

- 2006 : Start of the SDHCAL development with the aim to achieve the first technological prototype using the semi-digital readout concept;
- 2007 : Development of small detectors and associated electronics readout;
- 2008-2011 DHCAL ANR-blanc;
- 2010 : International review (organized by the IN2P3)
  CALICE internal review;
- 2011 : Construction of the SDHCAL prototype;
- 2012 : Test Beam at CERN;
- 2013 : Prototype data analyses and R&D for final validation of the SDHCAL-ILD.

Several groups of the CALICE collaboration contribute to the project :

France : IPNL, LAPP, LLR, LPC, OMEGA;
Spain : CIEMAT;
Belgium : UCL, Gent;
China : Tsinghua university, NCEPU;
Tunisia : Tunis university.

SDHCAL concept

1- Detector choice

Gaseous detectors: homogenous, cost-effective and highly transverse and longitudinal **granular**.

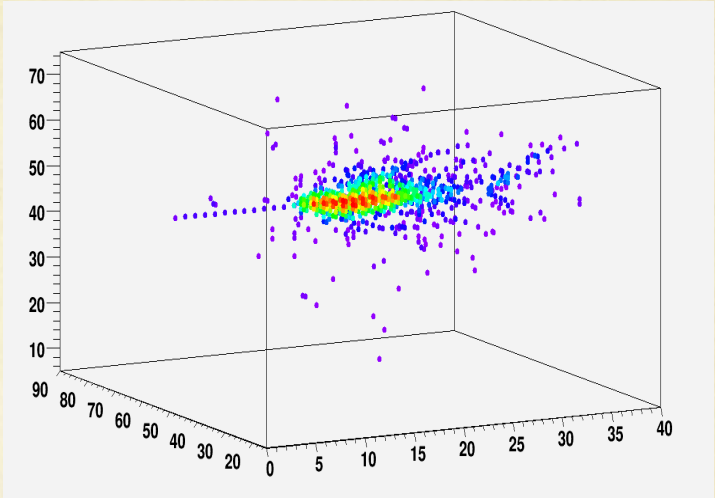
GRPC : is an adequate candidate for ILC.

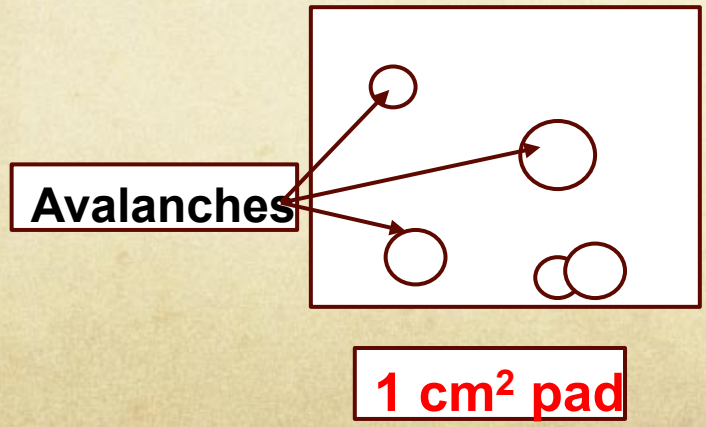
2- Electronics readout choice

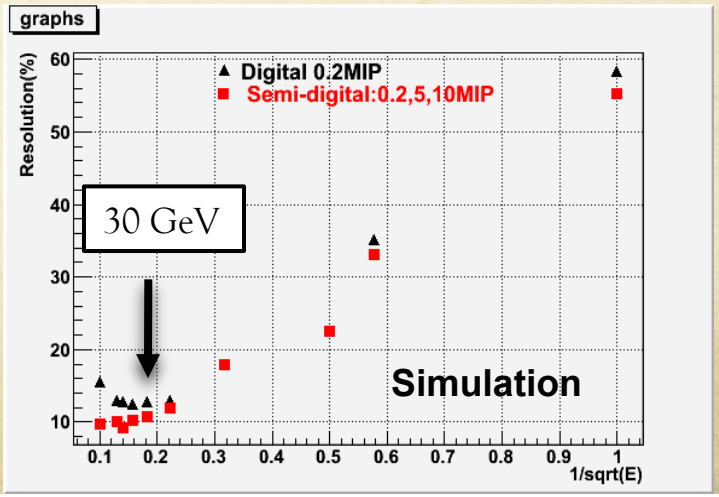
At high energy the shower core is very dense

→ Simple binary readout will suffer saturation effect

→ Semi-digital readout (2-bit) can improve the energy resolution.

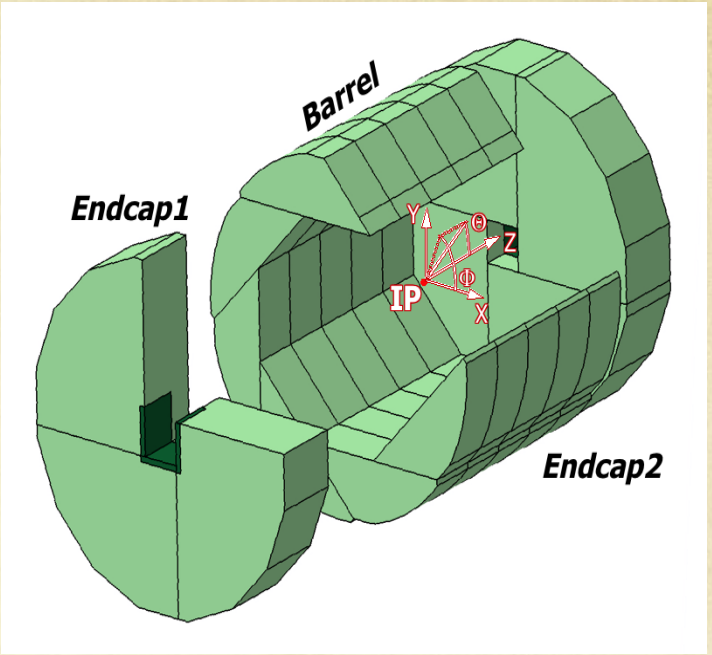






SDHCAL-ILD

The SDHCAL-GRPC is one of the two HCAL options proposed in the **ILD L**etter **O**f **I**ntention (LOI). Modules are made of 48 RPC chambers ($6\lambda_I$) equipped with power-pulsing electronics readout.



The structure proposed for the SDHCAL-ILD :

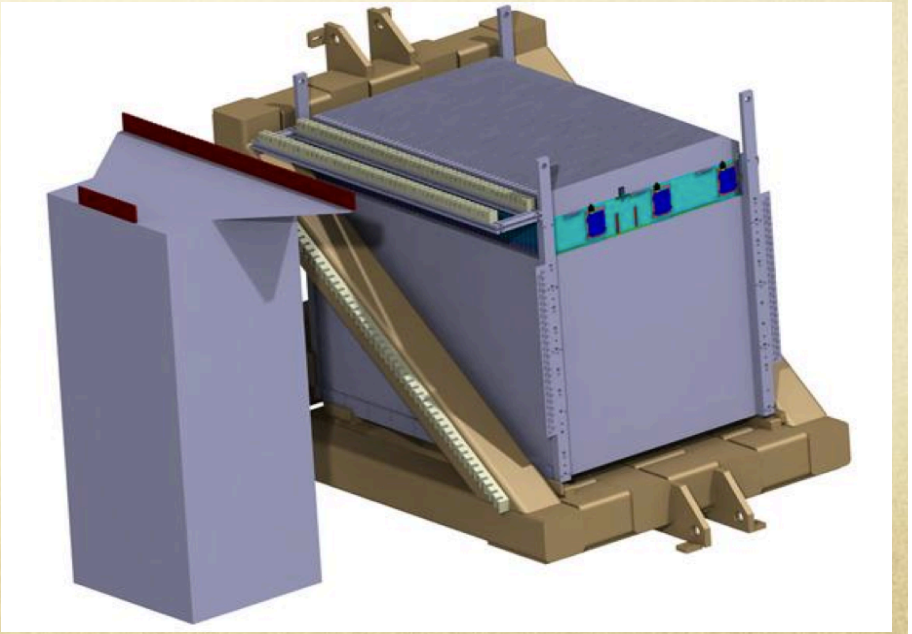
- Is self-supporting
- Has negligible dead zones
- Eliminates projective cracks
- Minimizes barrel / endcap separation (services leaving from the outer radius)

SDHCAL Prototype

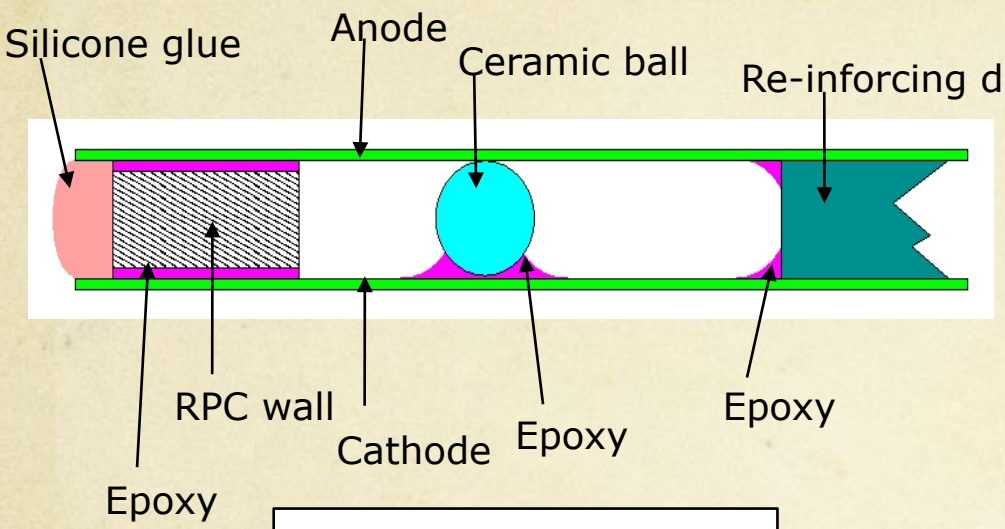
- Come as close as possible to the ILD module and be able to study hadronic showers
-48 units (active layer + absorber) fulfilling the ILD requirements.

Challenges

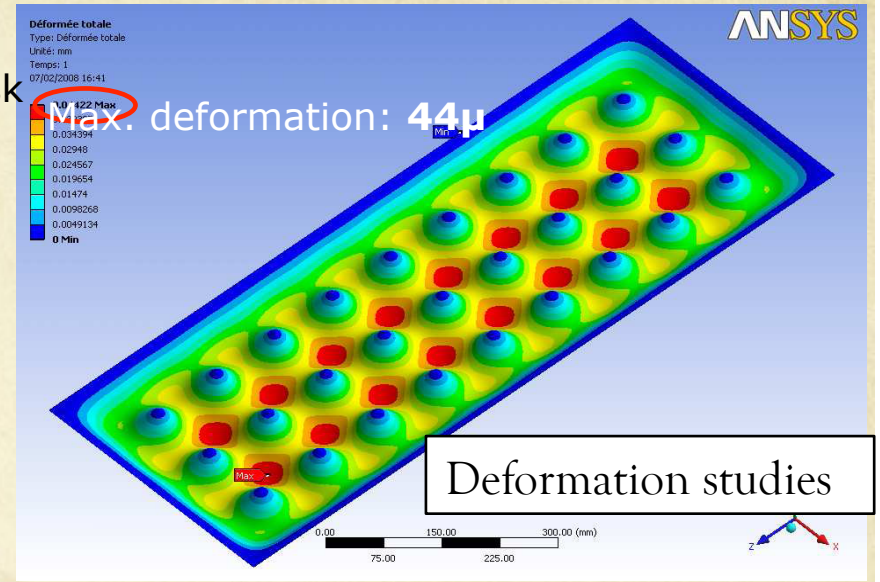
-Homogeneity for large surfaces
-Thickness of only few mms
-Services from one side
-Embedded power-cycled electronics
-Self-supporting mechanical structure



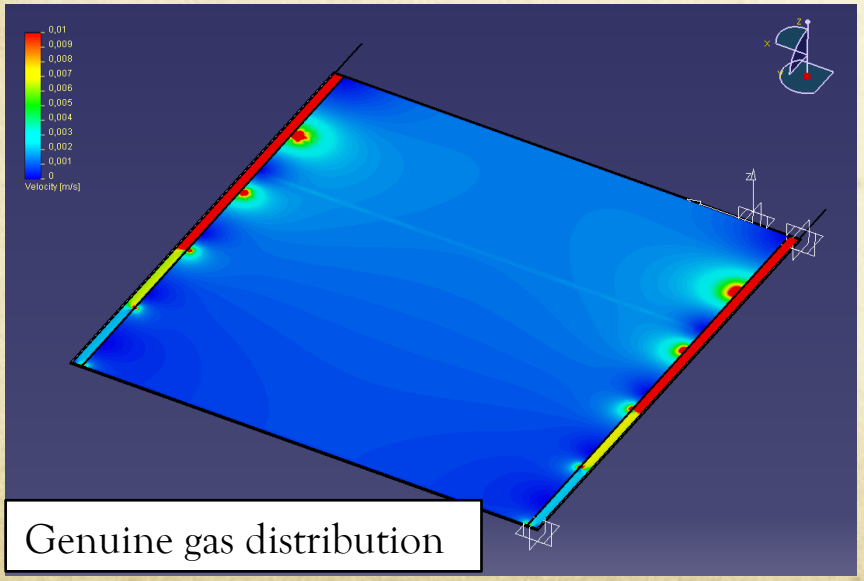
GRPC development



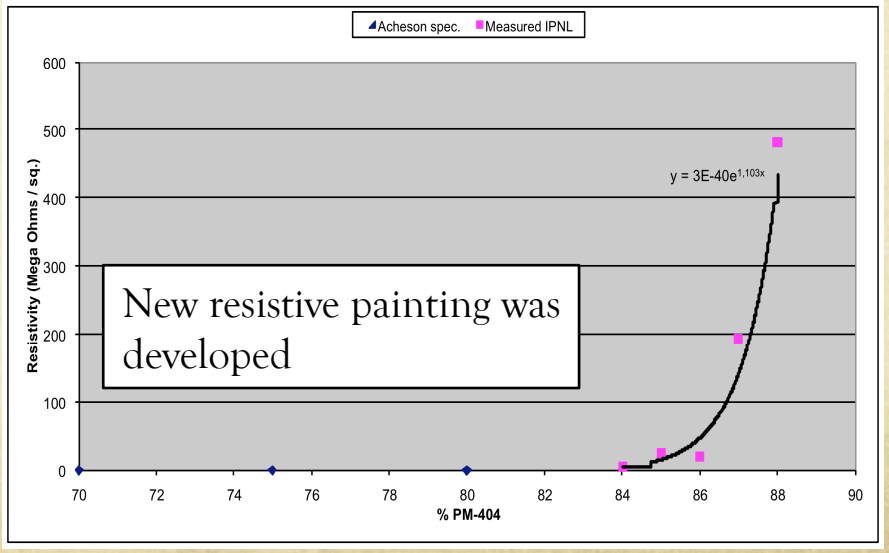
Dead zones minimized



Deformation studies



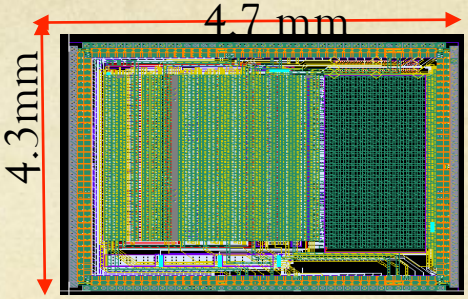
Genuine gas distribution

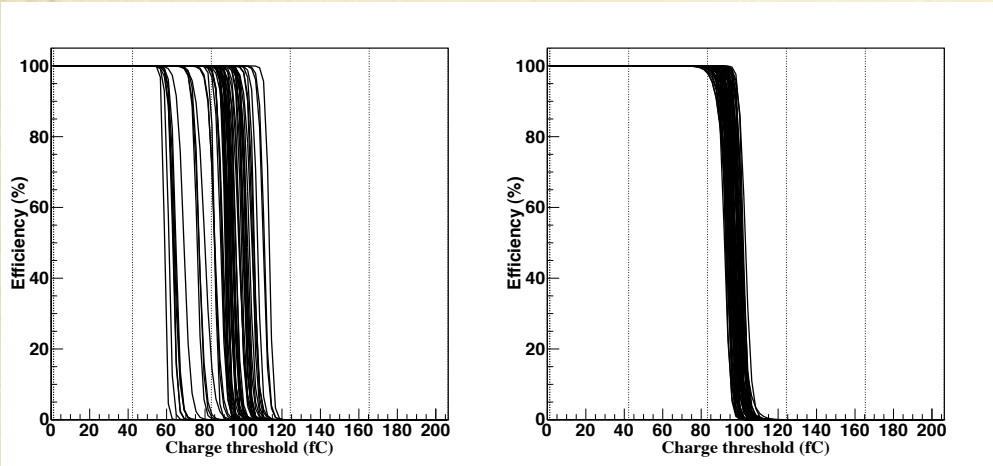


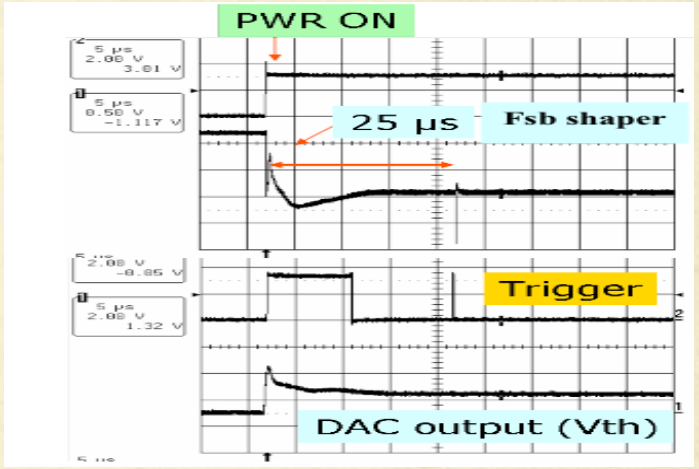
New resistive painting was developed

Electronics readout development

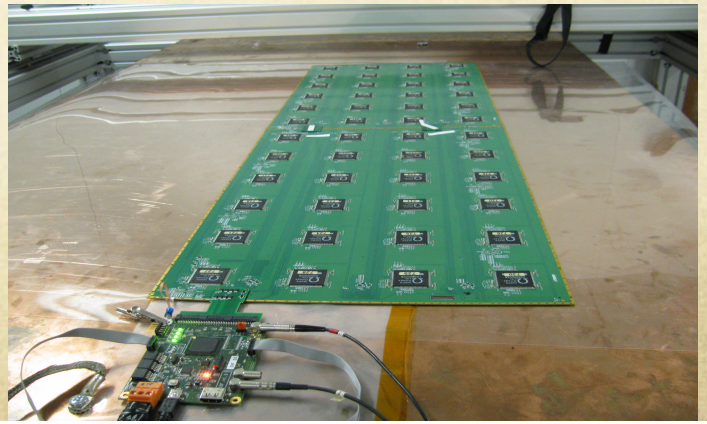
ASIC: HARDROC
64 channels, trigger less mode, memory depth: 127 events
2-bit readout : 3 thresholds
Dynamic range: 10 fC-15 pC
Gain correction → uniformity
Power-pulsed → reduced power consumption



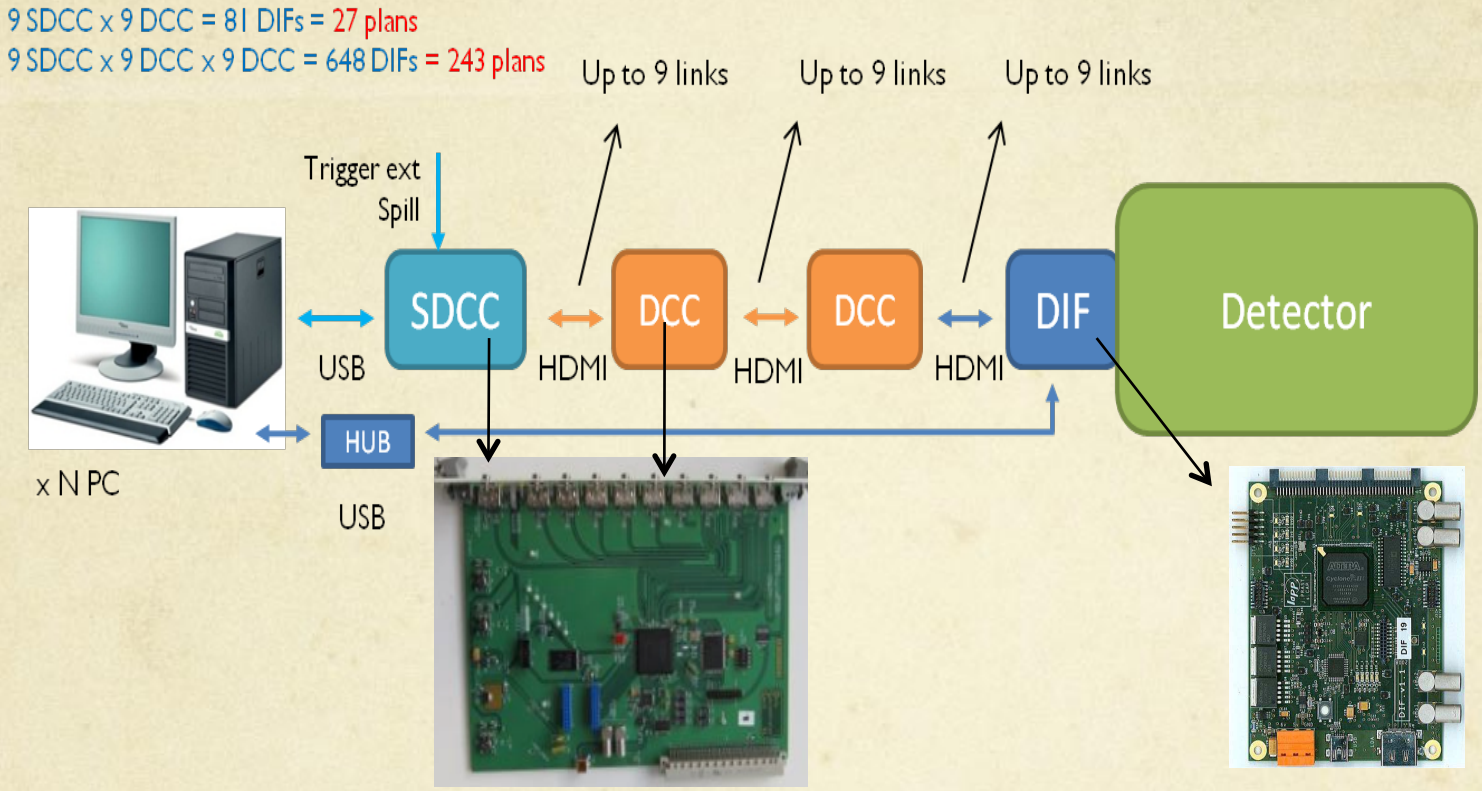




Printed Circuit Boards (PCB) were designed to reduce the x-talk with 8-layer structure and buried vias.
Tiny connectors were used to connect the PCB two by two (the 24X2 ASIC are daisy-chained).
DAQ board (DIF) was developed to transmit fast commands and data to/from ASICs.



SDHCAL acquisition system



→ Acquisition software was developed to deal with the output of large number of electronics channels (> 460 000).

→ Oracle database used for ASIC configurations and slow control.

→ CMS Xdaq used to provide the DAQ framework.

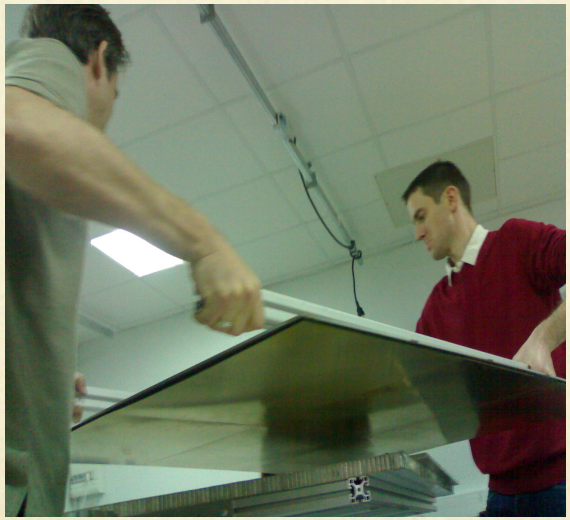
Cassette development

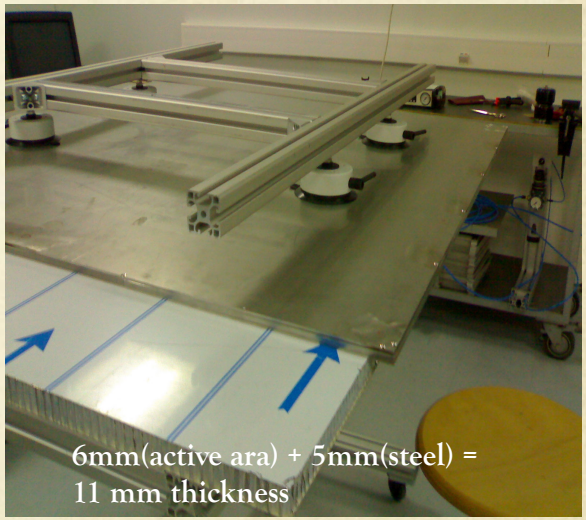
→ To provide a robust structure.

→ To maintain good contact between the readout electronics and the GRPC.

→ To be part of the absorber.

→ It allows to replace detectors and electronics boards easily.

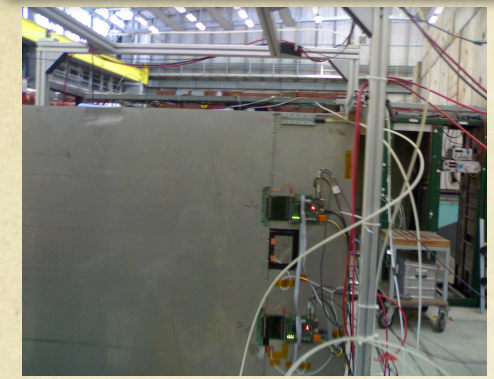


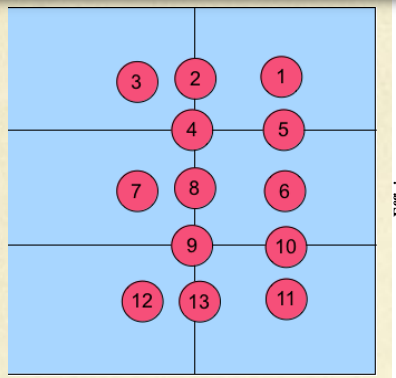


The cassettes are built of no-magnetic stainless steel walls 2.5 mm thick each → Total cassette thickness = 6mm (active layer)+5 mm (steel) = 11 mm

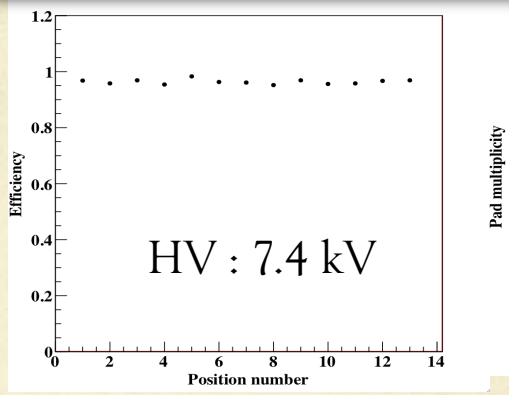
Test Beam validation

The homogeneity of the detector and its readout electronics were studied

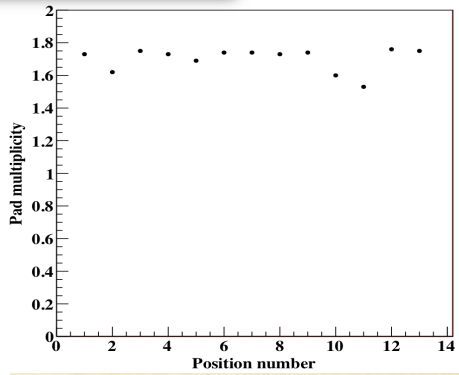




Beam spot position

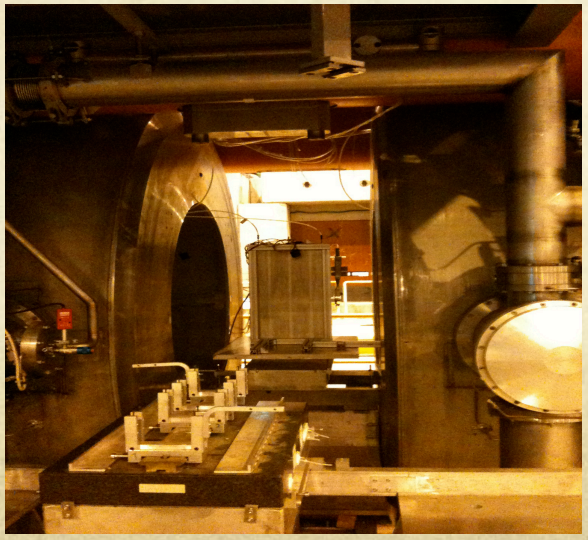


Efficiency

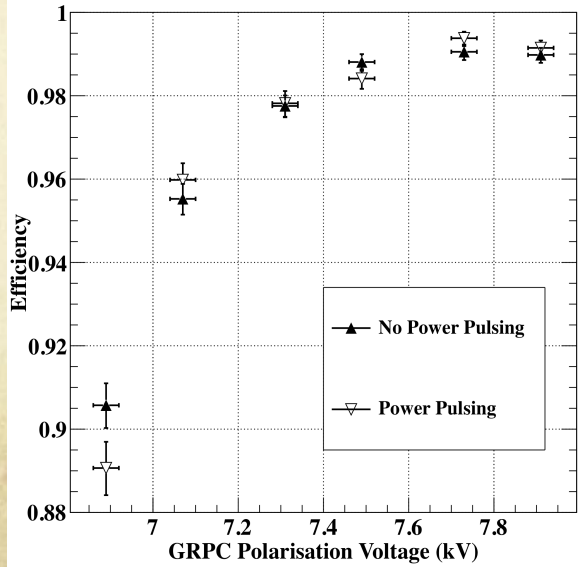


Multiplicity

Power-Pulsing mode was tested in a magnetic field of 3 Tesla

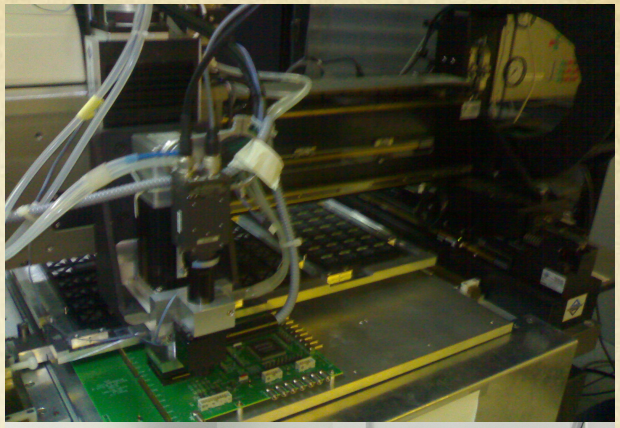


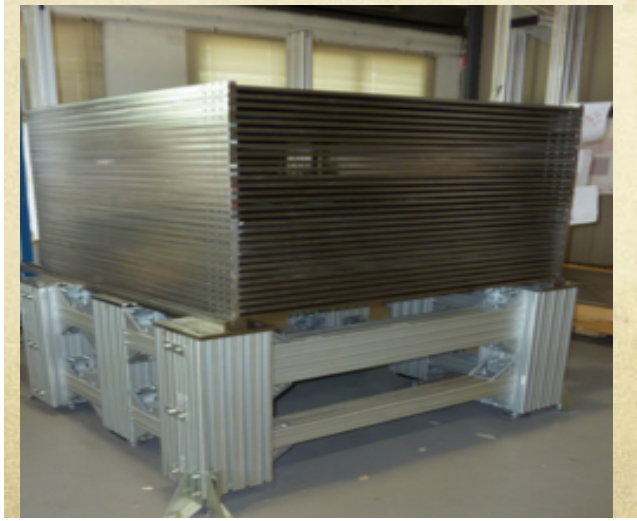
The Power-Pulsing mode was applied on a GRPC in a 3 Tesla field at H2-CERN (2ms every 10ms)
No effect on the detector performance

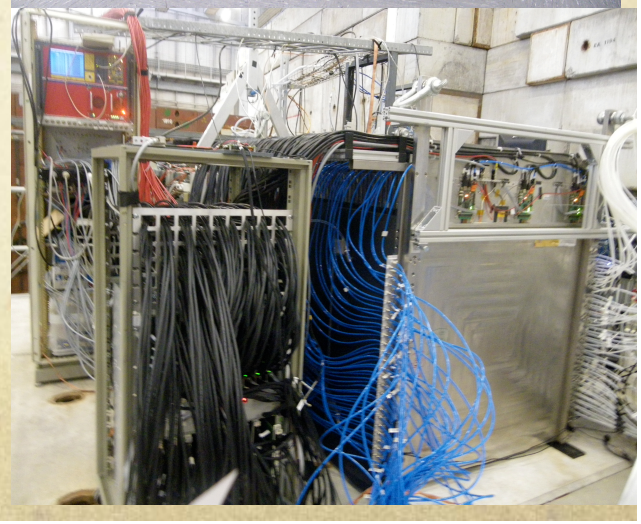


SDHCAL prototype construction

- ✓ 10500 ASIC were tested and calibrated using a dedicated robot that was used by CMS (IPNL, OMEGA) (ASICs layout : 93%).
- ✓ 310 PCBs were produced, cabled and tested (IPNL). They were assembled by sets of six to make 1m^2 ASUs
- ✓ 170 DIF(LAPP), 20 DCC(LLR) were built and tested.
- ✓ 50 detectors were built and assembled with their electronics into cassettes. Cassettes were tested by sets of 6 using a cosmic test bench (IPNL).
- ✓ The mechanical structure was built in CIEMAT.
- ✓ HV, cooling services were built by UCL, Gent.
- ✓ Full assembly took place at CERN.







Prototype @TB

3 periods of TB in 2012 (5 weeks)

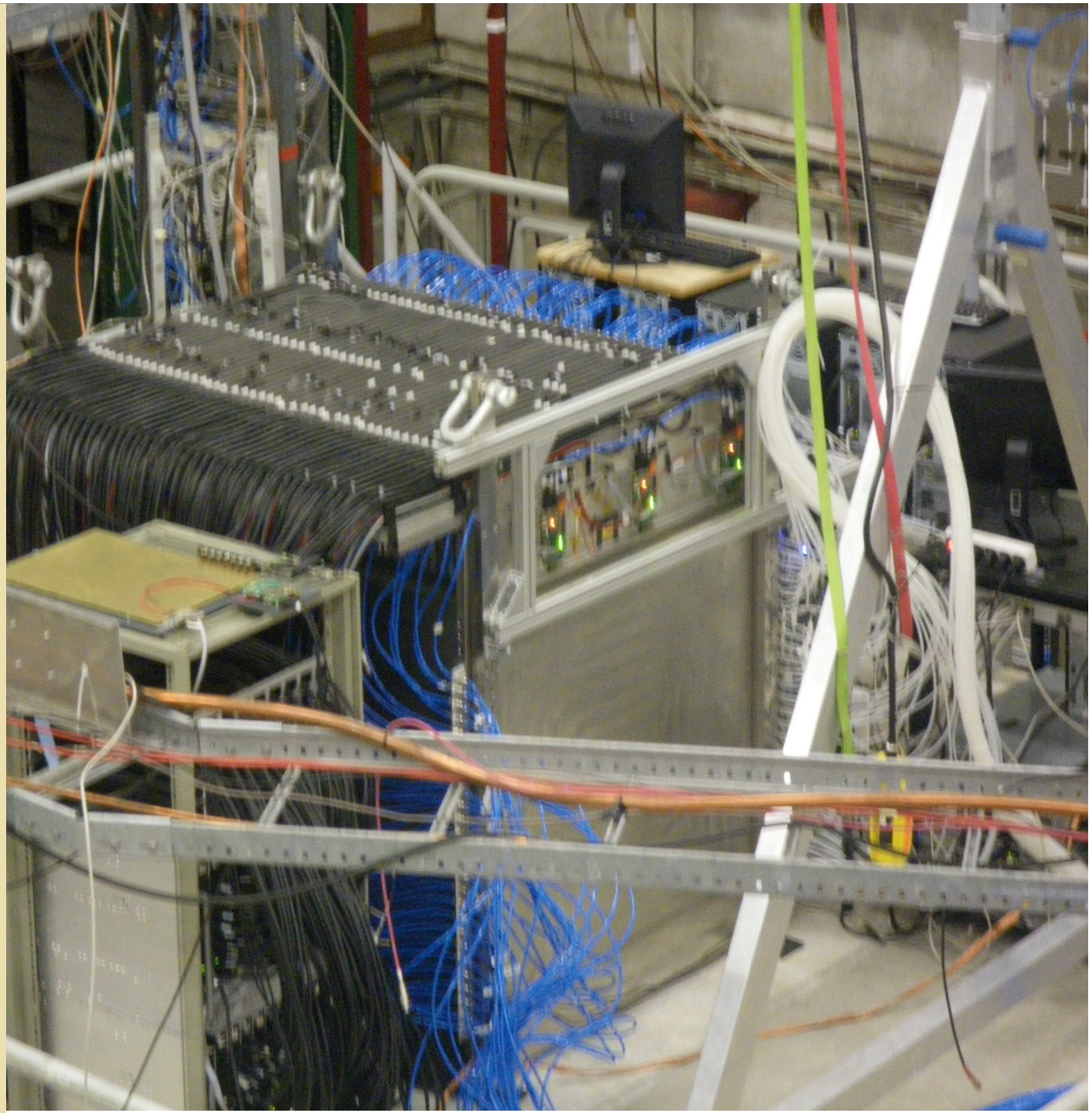
→ SDHCAL Commissioning with Power-Pulsing

→ Thresholds choice optimization

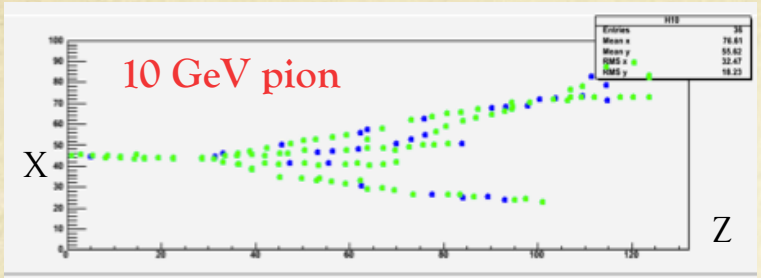
→Muons run calibration

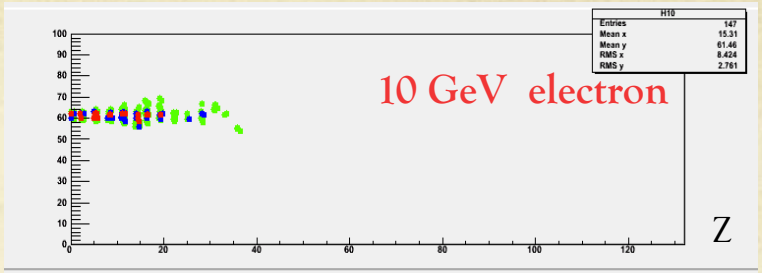
→ Pion, electron runs to study EM and hadronic showers

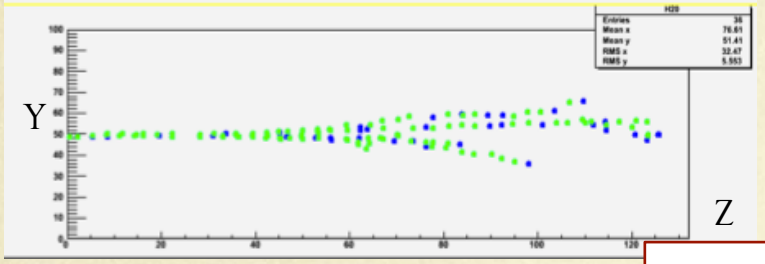
→No particle identification detector was used

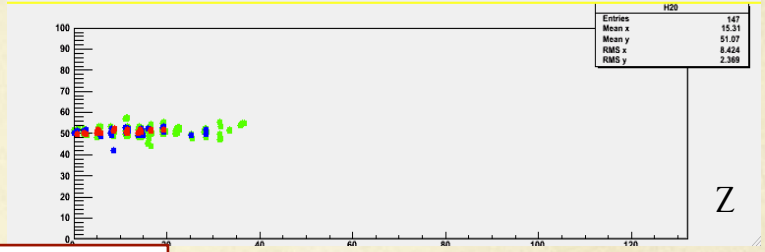


Event display



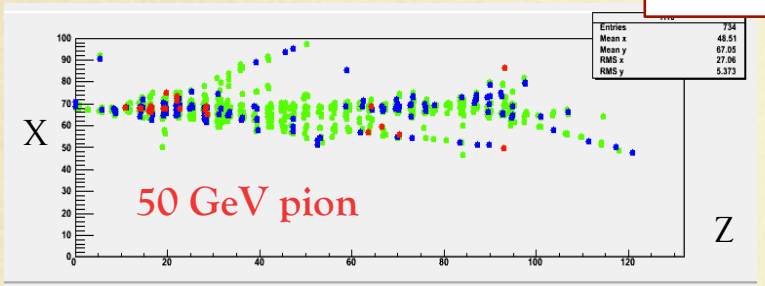


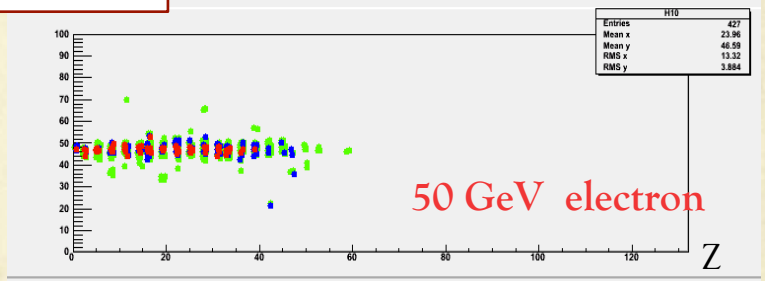


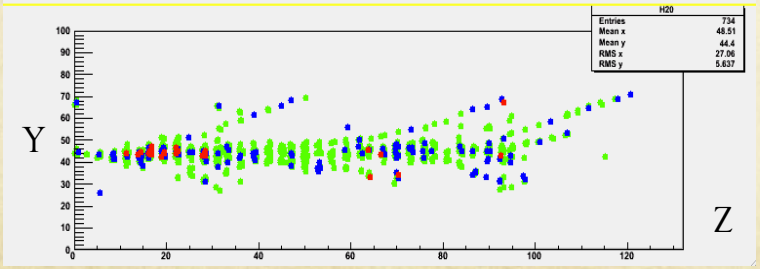


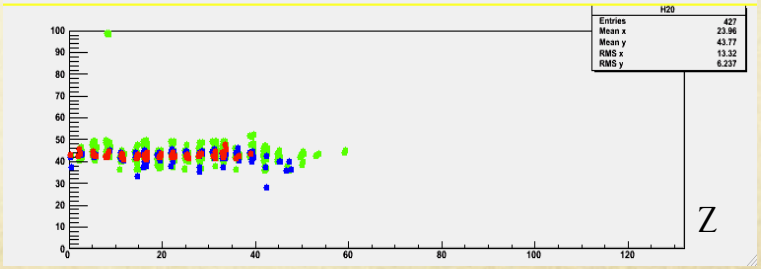
Power-Pulsed

units in cm









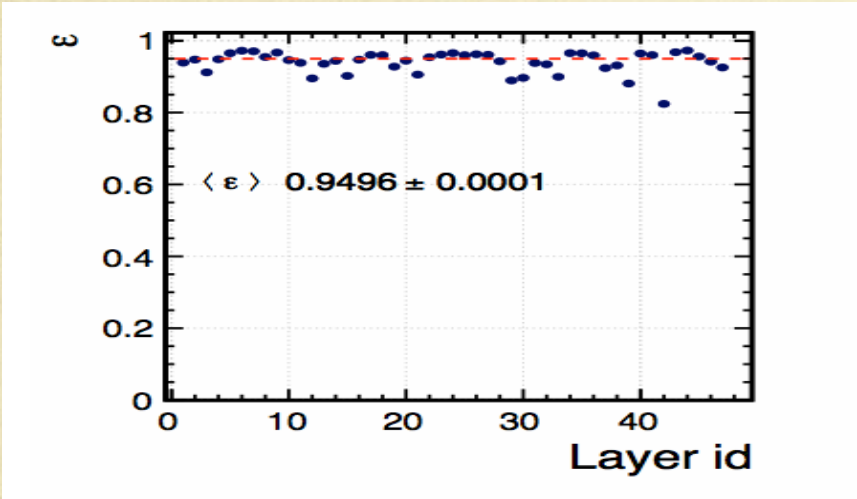
Colours correspond to the three thresholds: Green (100 fC), Blue (5 pC), Red (15 pC)

Raw data, no treatment except time hit clustering

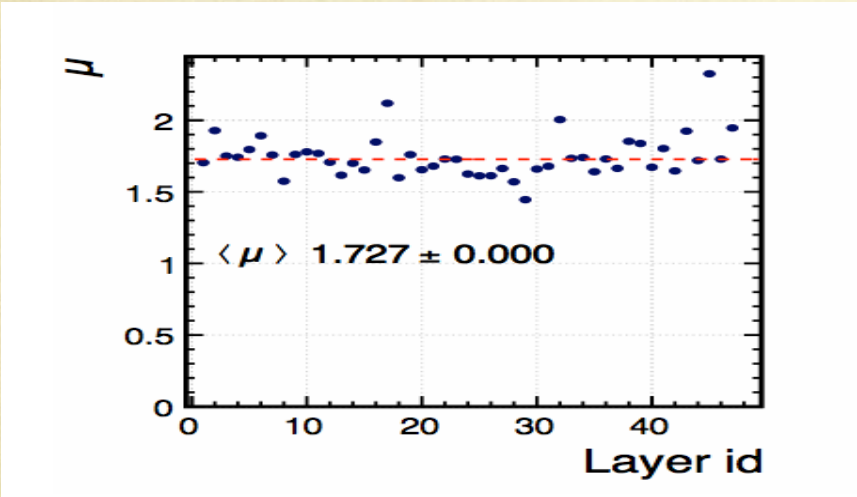
First results on linearity and energy resolution

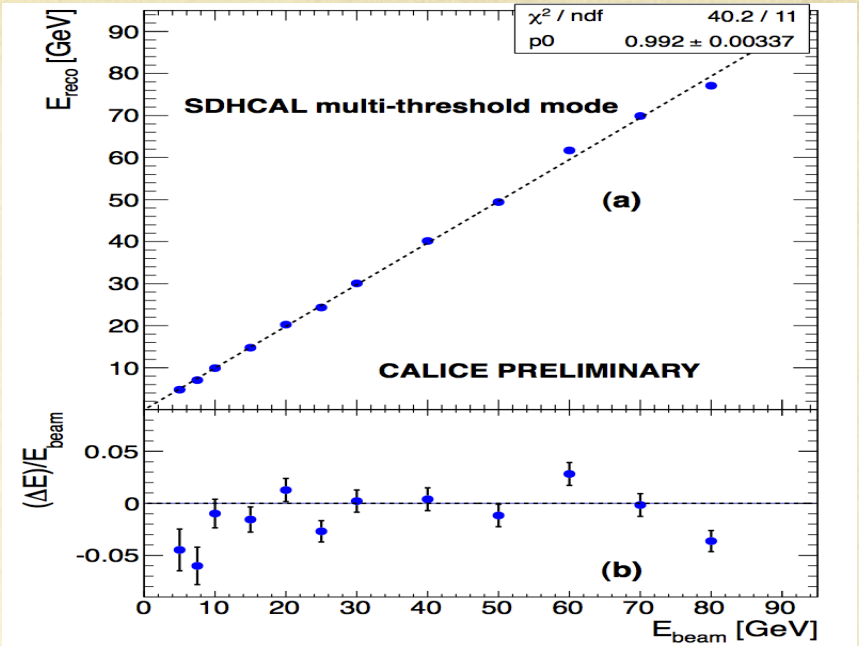
with no calibration and with no gain correction.

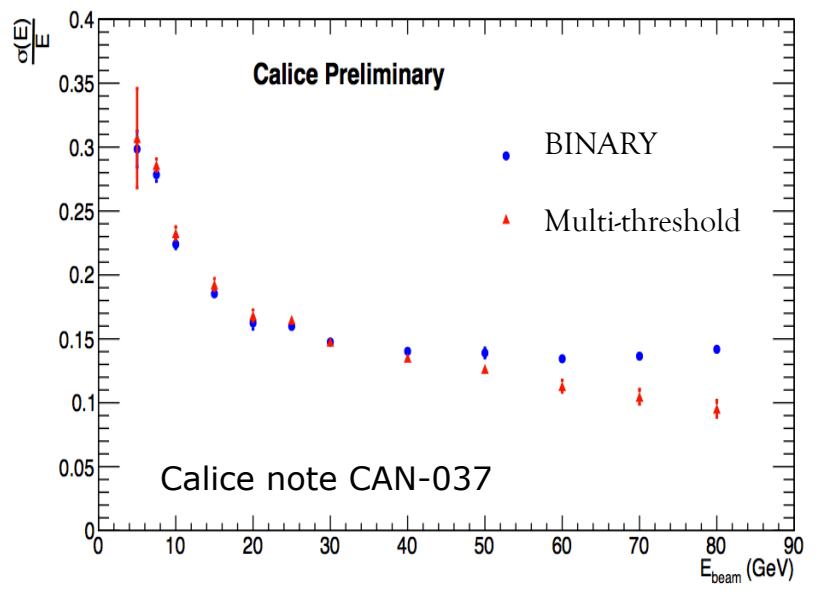
Efficiency



Pad multiplicity







Semi-digital improvement with respect to digital version.

Ongoing analyses

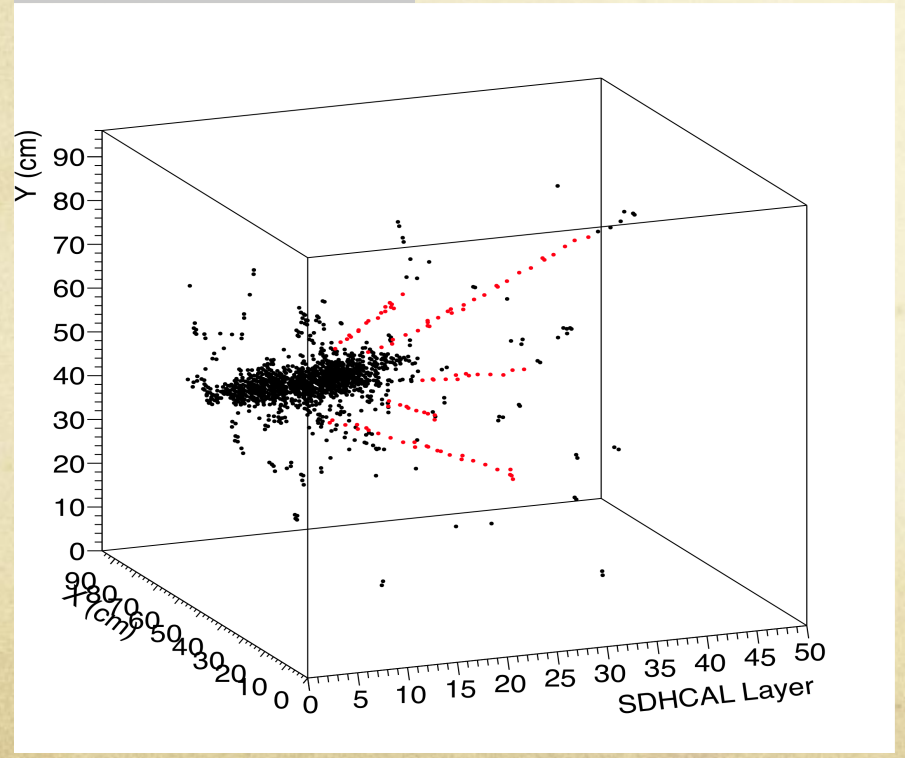
→ Calibration study

→ Electron-Pion separation

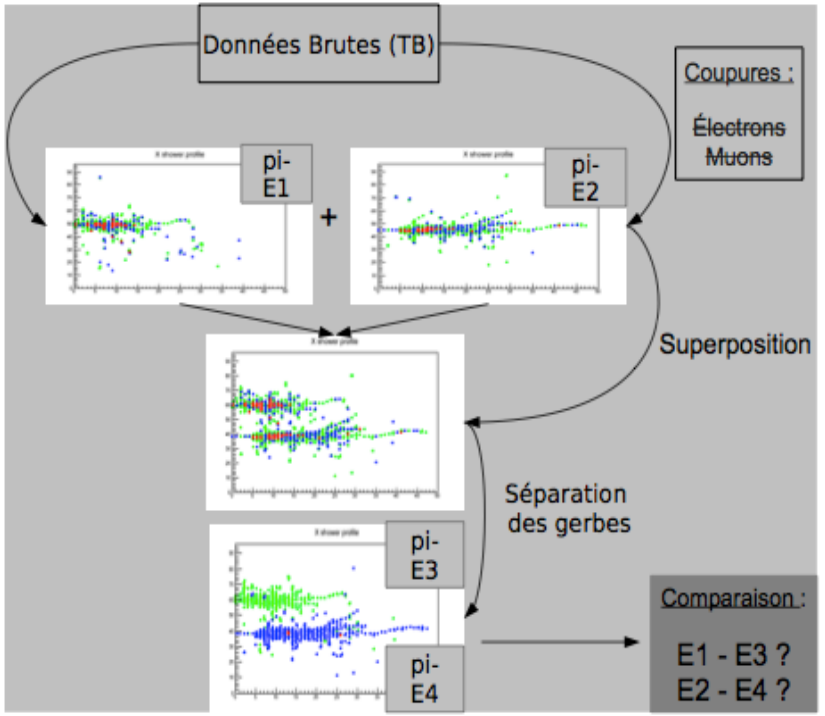
→ Energy resolution improvement by taking into account hadronic shower structure and calibration correction.

→ Imaging algorithm developments (HT, Arbor, MST) → PFA

Hough Transform

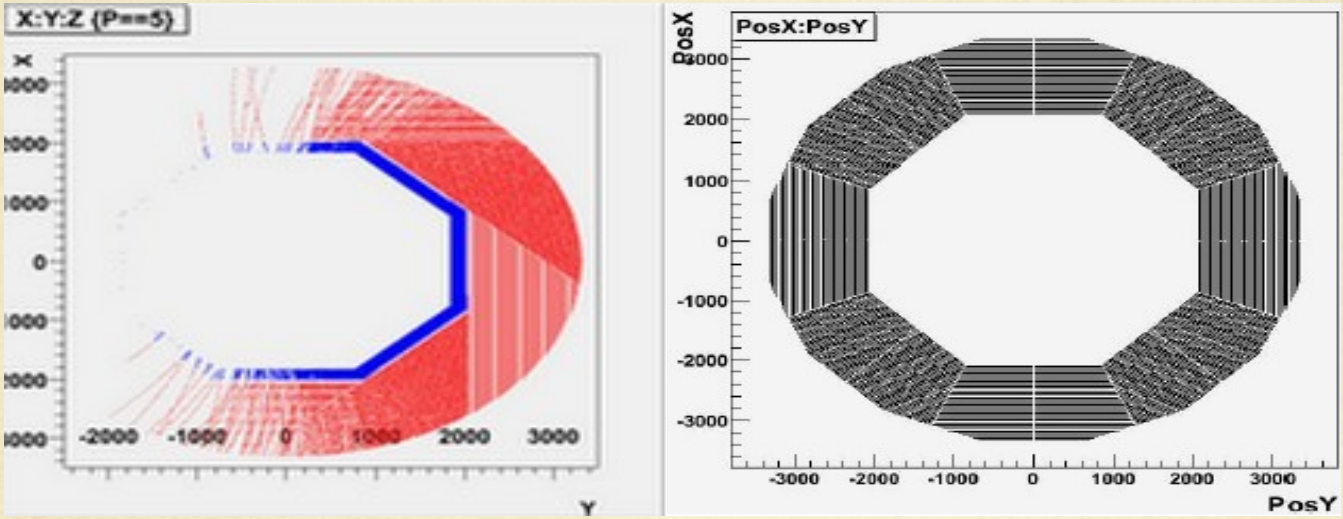


Arbor, MST..

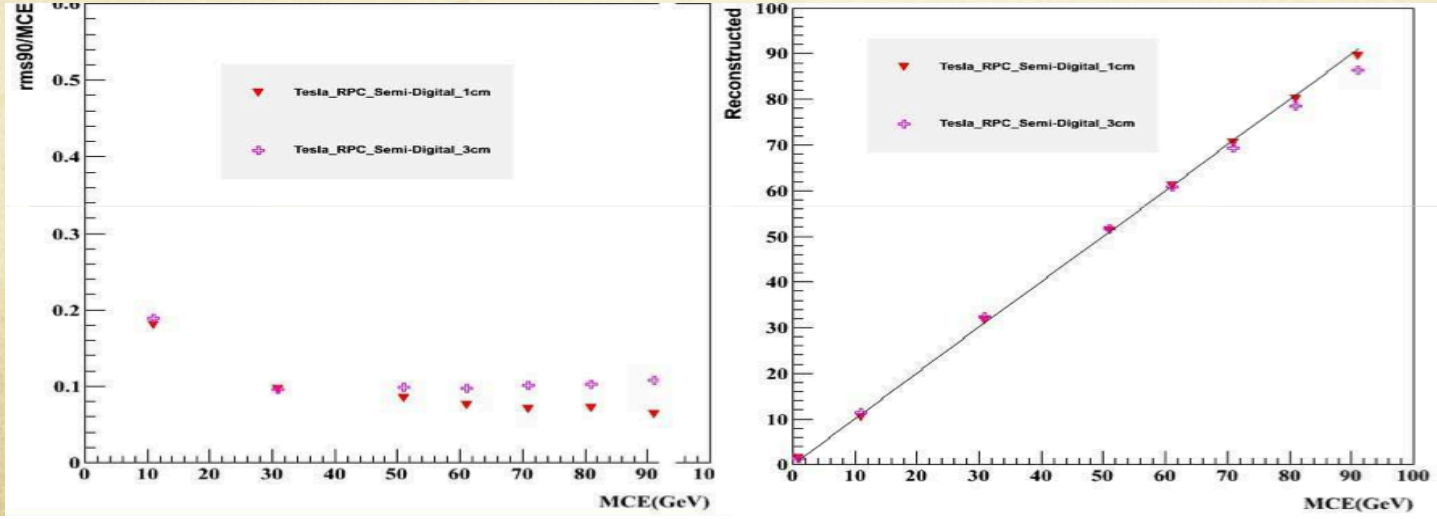


Simulation and optimization studies

SDHCAL was simulated with two mechanical structures for ILD (V and Tesla)



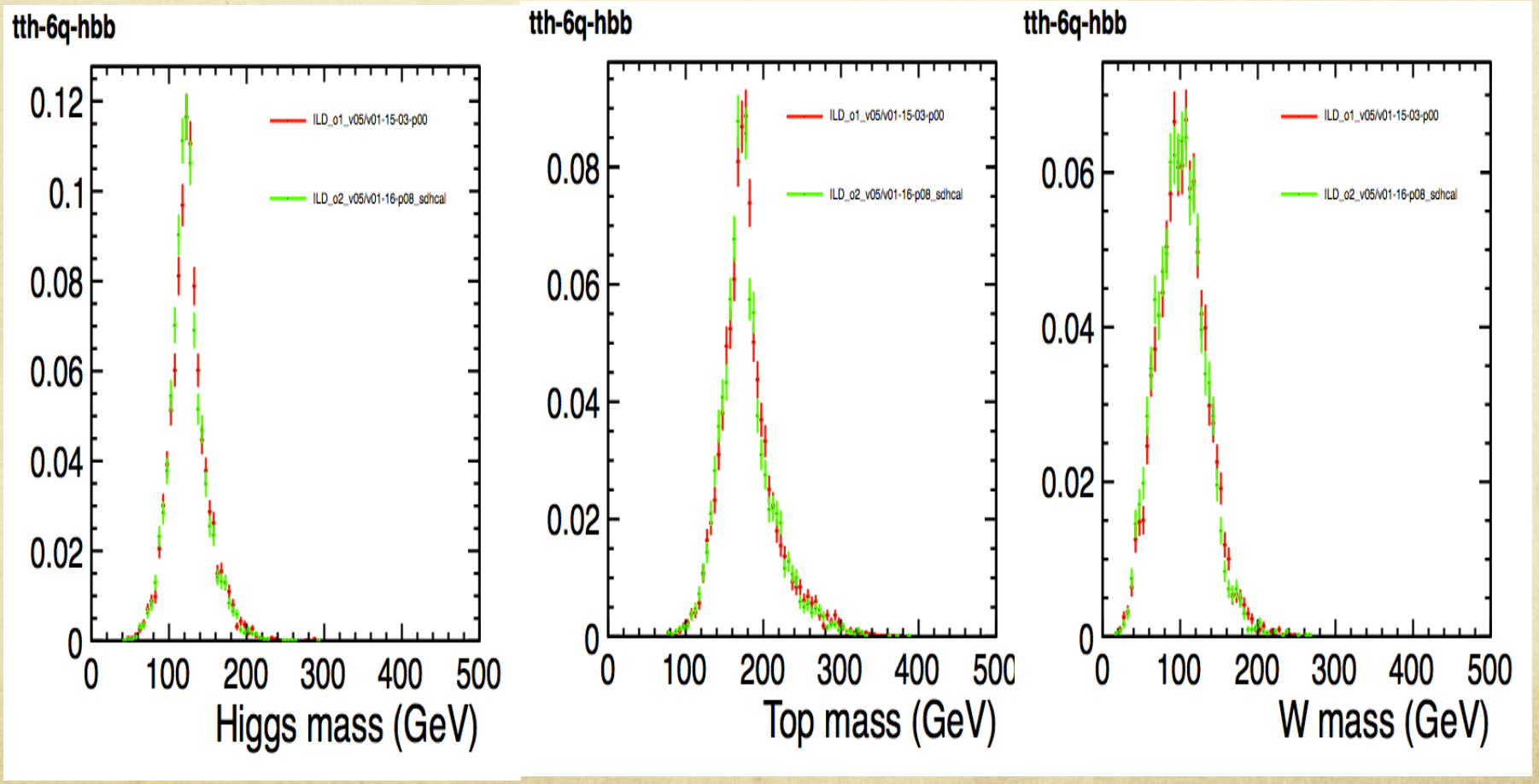
Studies on granularity and readout (binary vs semi-digital) were conducted. They allowed to confirm the SDHCAL choice before to start building the prototype



Simulation and optimization studies

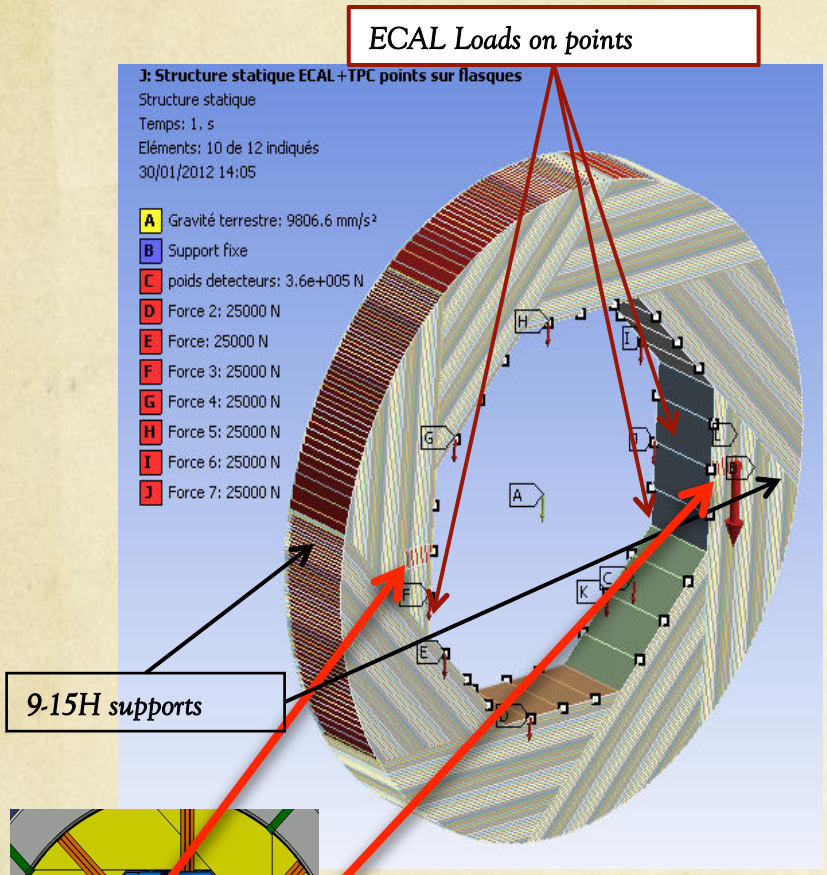
The SDHCAL simulation was re-performed taking into account the constraints and the results of the prototype. The new version was used for the DBD studies, showing that same performance are obtained as for the AHCAL (albeit the PFA optimization was done for the AHCAL topology)

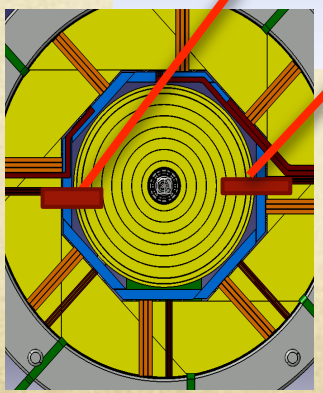
Higgs, top and W in the tth 8jet mode (1000 GeV).



Tomohiko Tanabe

Mechanical, integration, service studies

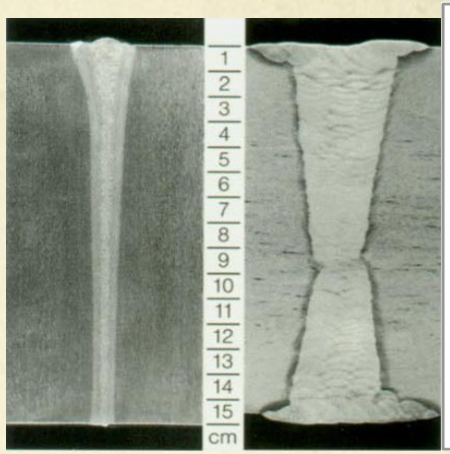


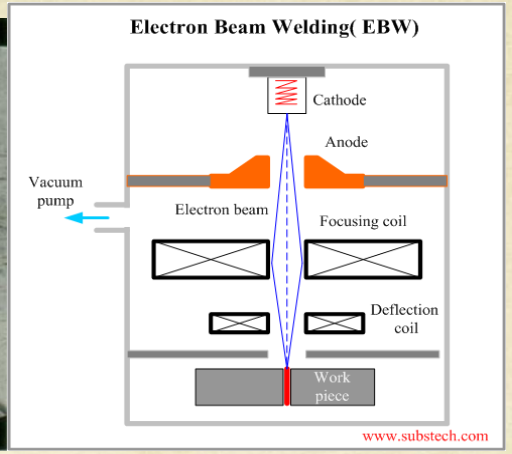


DHCAL with 8 x ECAL modules (8x2.5 t)

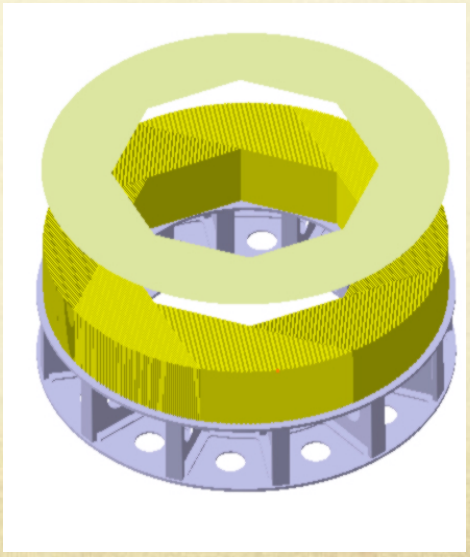
And TPC (4t)

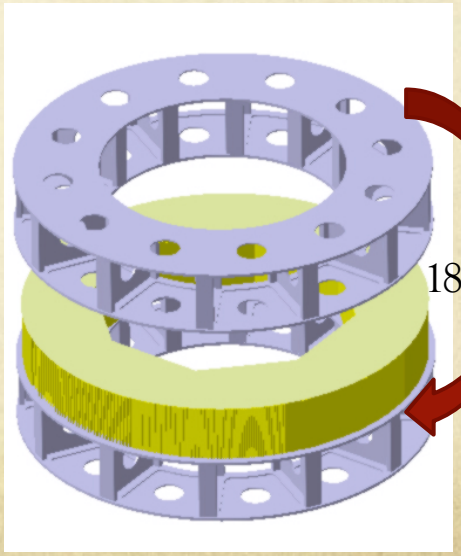
Welding techniques





Building scenarios

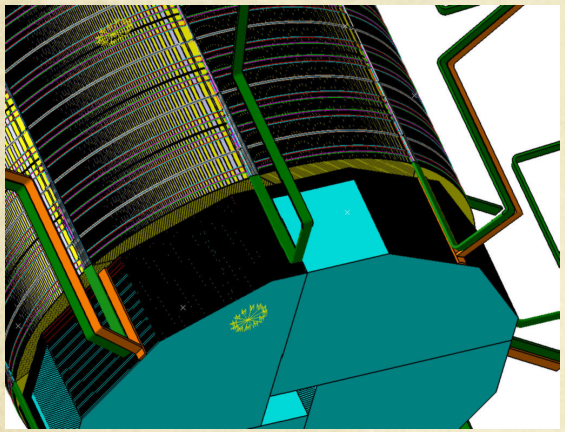


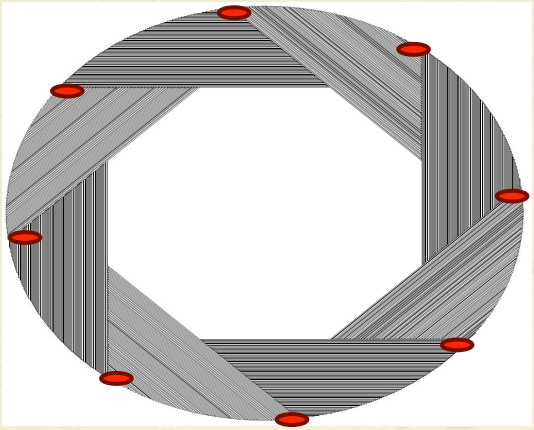


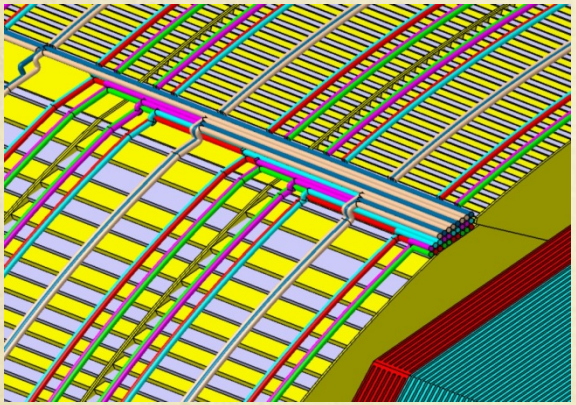
Deformation max SDHCAL + ECAL + TPC = 0,4 mm

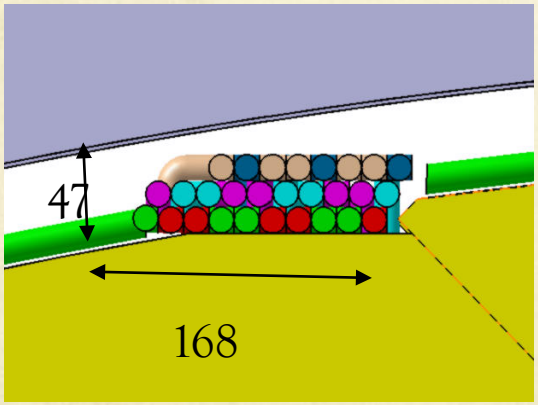
Mechanical, integration, service studies

Services were studied in detail to provide a realistic model for the ILC DBD

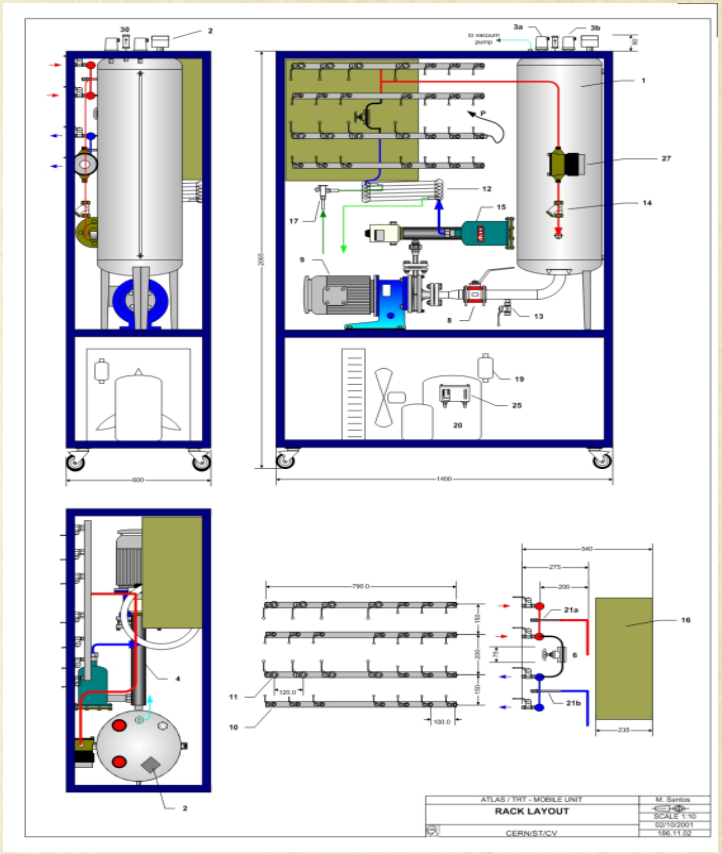








Few cooling scenarios were studied and compared with each other



Mono-phasic gas like C6F14 : limited effect in case of leak, good quality/price ratio, adapted to low heat extract, simple to use

Road map in the 2-3 coming years

-Improve on the energy reconstruction using new techniques;

-Develop PFA techniques to be used to separate close-by hadronic showers;

-Build few very large GRPC detectors (2-3 m2) : gas circulation system, thickness…

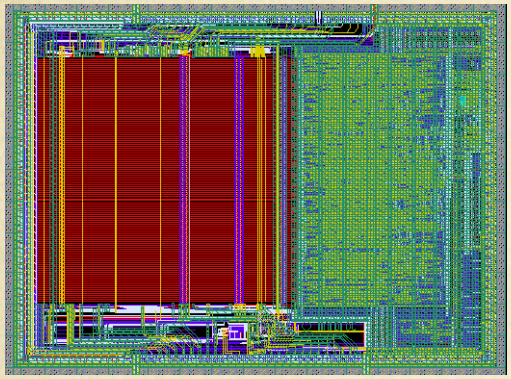
-Improve on the electronics (I2C, roll mode..);

-Design a new ASU capable to read the large GRPC (up to 3 m^2);

-Develop a new DIF (low consumption, reduced size, new functionalities);

- Build a small mechanical prototype to host the few large chambers.

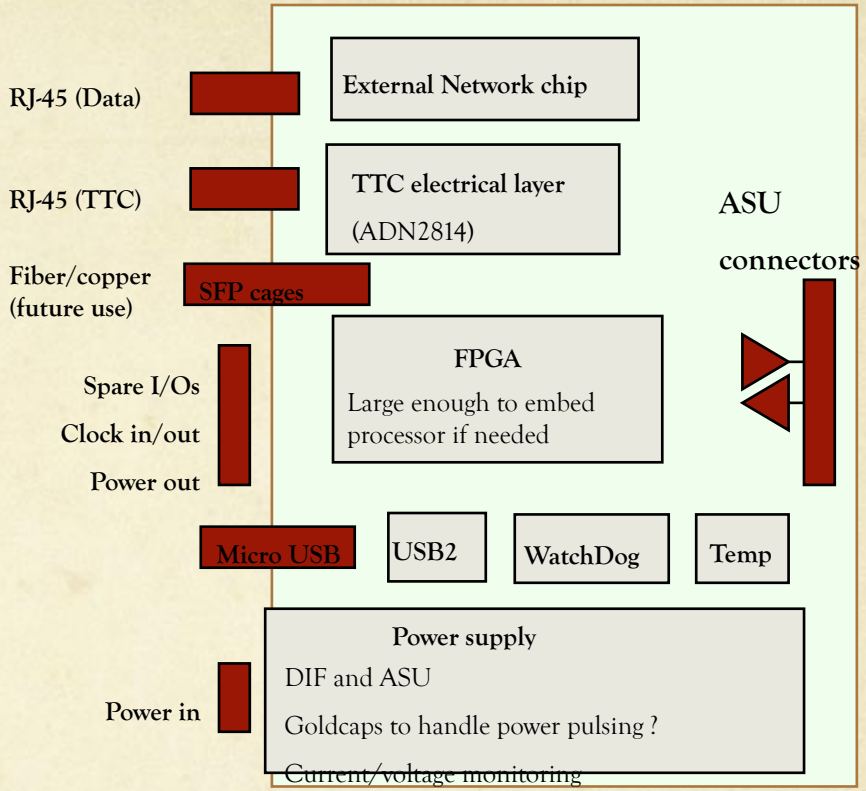
New version of the readout electronics



The new version improves on the previous one:
→Independent channels and zero suppression
→Independent ASICs (I2C)
→Better dynamic range (up to 50 pC).
This activity is funded essentially by **AIDA**

New ASU design for large detectors under study

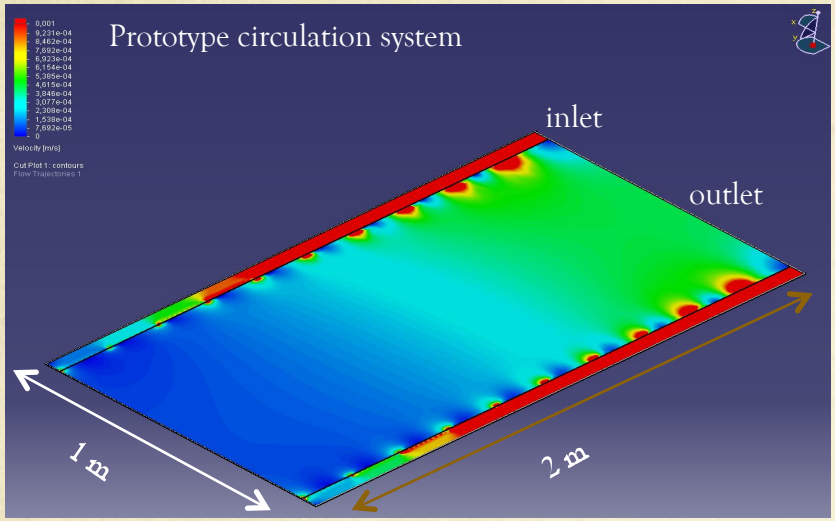
New features in the DAQ boards

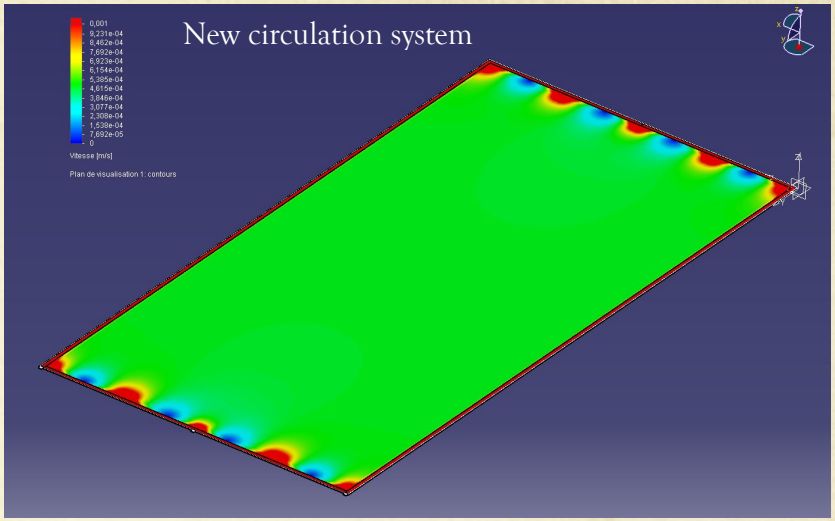


→ Only one DIF per plane. For the maximum length plane (1x3m) the DIF will handle 432 HR3 chips
→ Slow control through the new HR3 I2C bus
→ Data transmission to DAQ by Ethernet using commercial switches for concentration
→ Clock and synchronization by TTC

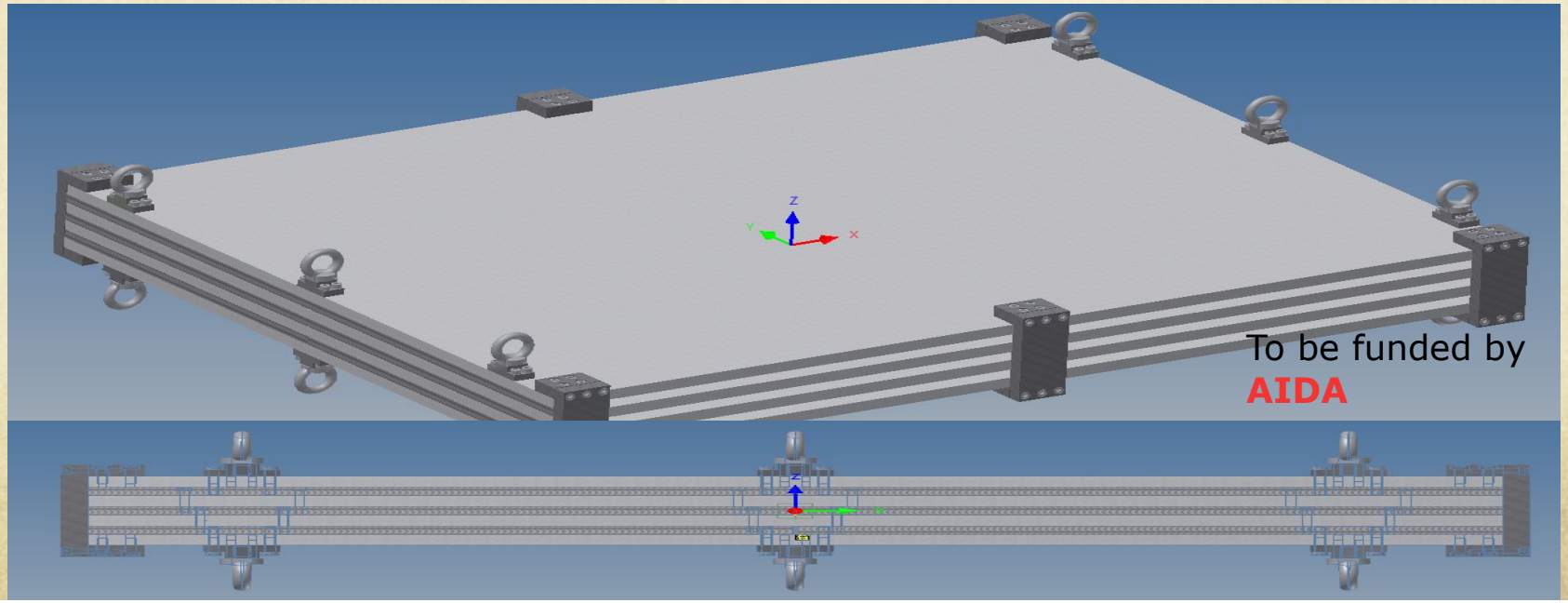
Funded essentially by CIEMAT

Detector improvement to achieve same performances with very large GRPCs





Mechanical structure to be built with EBW techniques and to host few large detectors GRPCs



Conclusion and prospects

-The SDHCAL prototype success proves that SDHCAL is a serious option for ILD;

-SDHCAL with its fine granularity is an excellent tool to develop and exploit PFA algorithms;

-The expertise accumulated during the conception, construction and commissioning is very precious for physicists and technical staff in our labs;

-The SDHCAL project is an excellent environment for students;

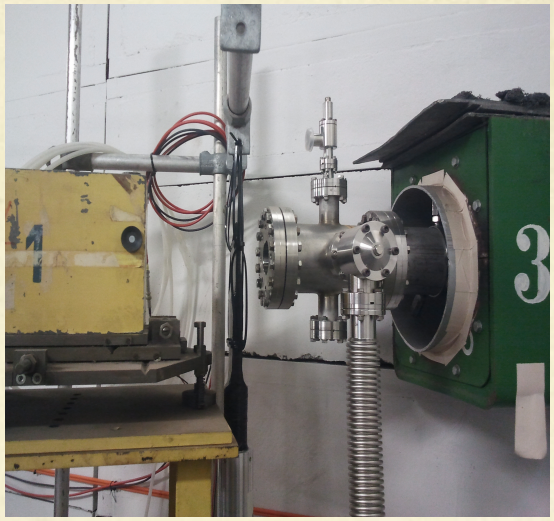
-The project has led to several spin-offs (TOMUVOL, CMS);

-We still need support from the IN2P3 to exploit the SDHCAL data and to finish the R&D (relatively modest in cost) to completely validate the SDHCAL option.

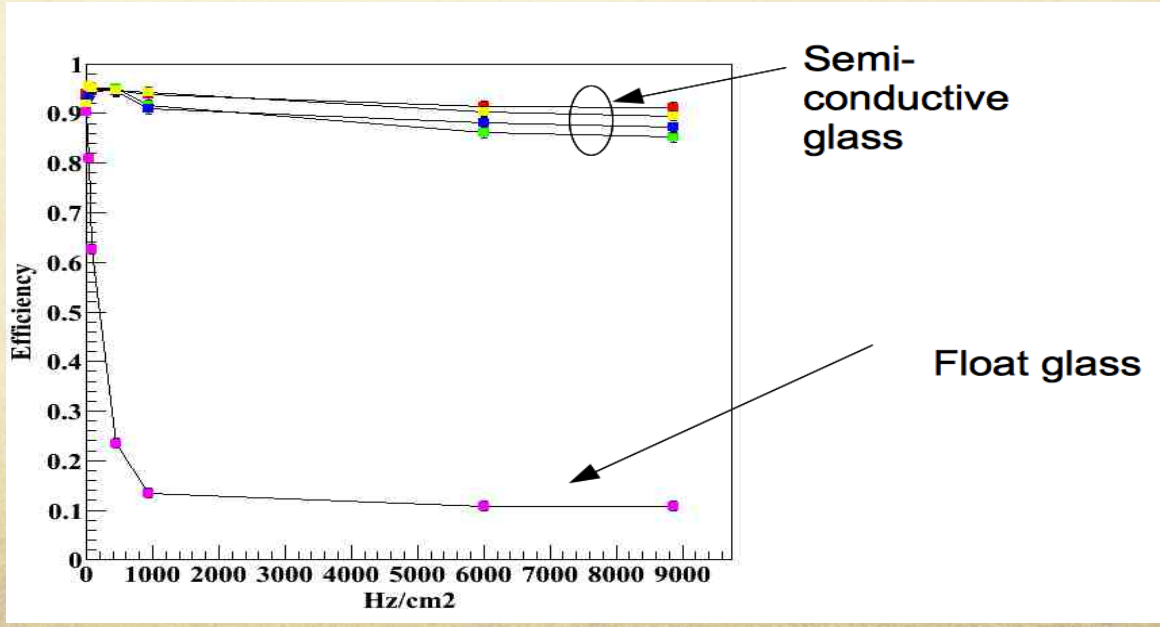
High-Rate GRPC

High-Rate GRPC may be needed in the very forward region

✓Semi-conductive glass (10^{10} Ω.cm) produced by our collaborators from Tsinghua University was used to build few chambers.
✓4 chambers were tested at DESY as well as standard GRPC (float glass)

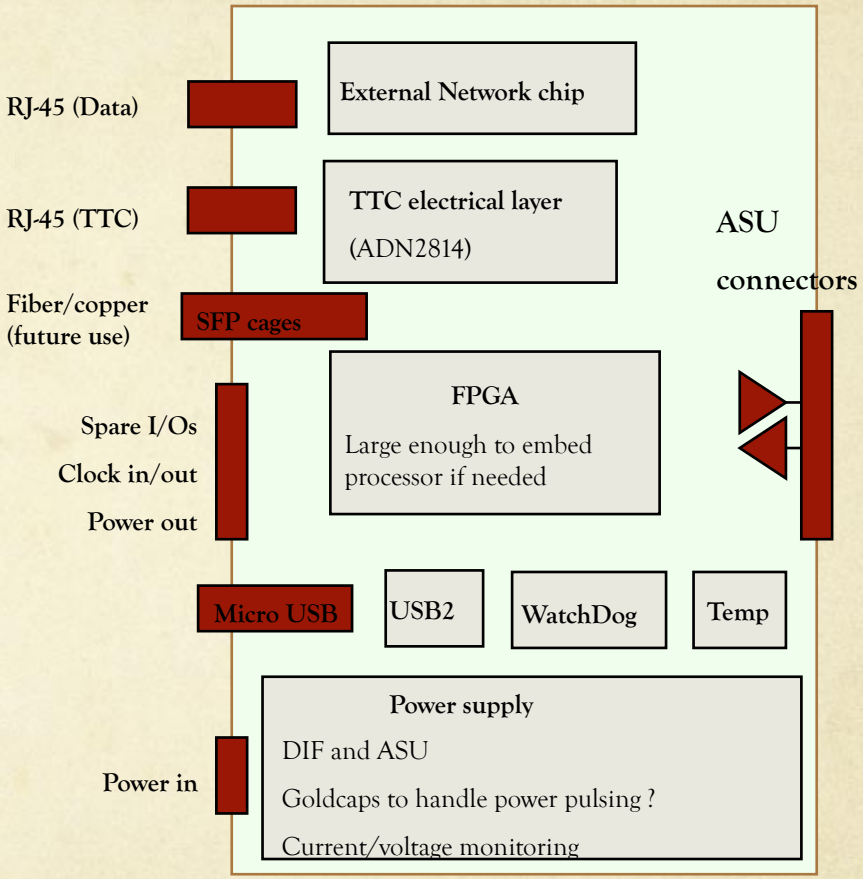


Performance is found to be excellent at high rate for GRPCs with the semi-conductive glass and can be used in the very forward of ILD region if the rate exceeds 100 Hz/cm^2 in future ILD upgrades



DIF: Designed for ILD SDHCAL

- Only one DIF per plane. For the maximun lenght plane (1x3m) the DIF will handle 432 HR3 chips
- Slow control through the new HR3 I2C bus
- Data transmision to DAQ by Ethernet using comercial switches for concentration
- Clock and syncronization by TTC
- USB 2.0 for debugging



CIEMAT-IPNL

HARDROC3

I2C link (@IPNL)

PLL: integrated before in a builiding block, first measurements are very good

Input frequency 2.5 MHz =>output frequency: 10, 20, 40, and 80 MHz available

Bandgap: new one with a better temperature sensitivity, tested in a building block

Roll mode

Triple voting

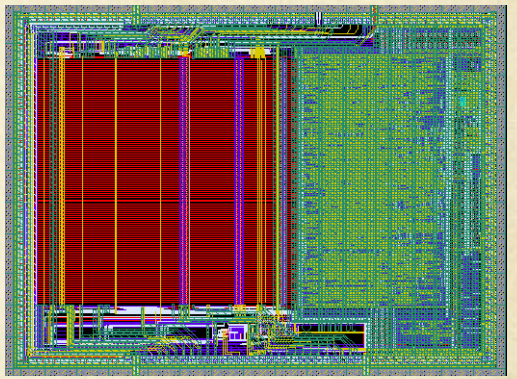
Temperature sensor: tested in a building block, slope – 6mV/°C

Die size ~30 mm2 (6.3 x 4.7 mm2)

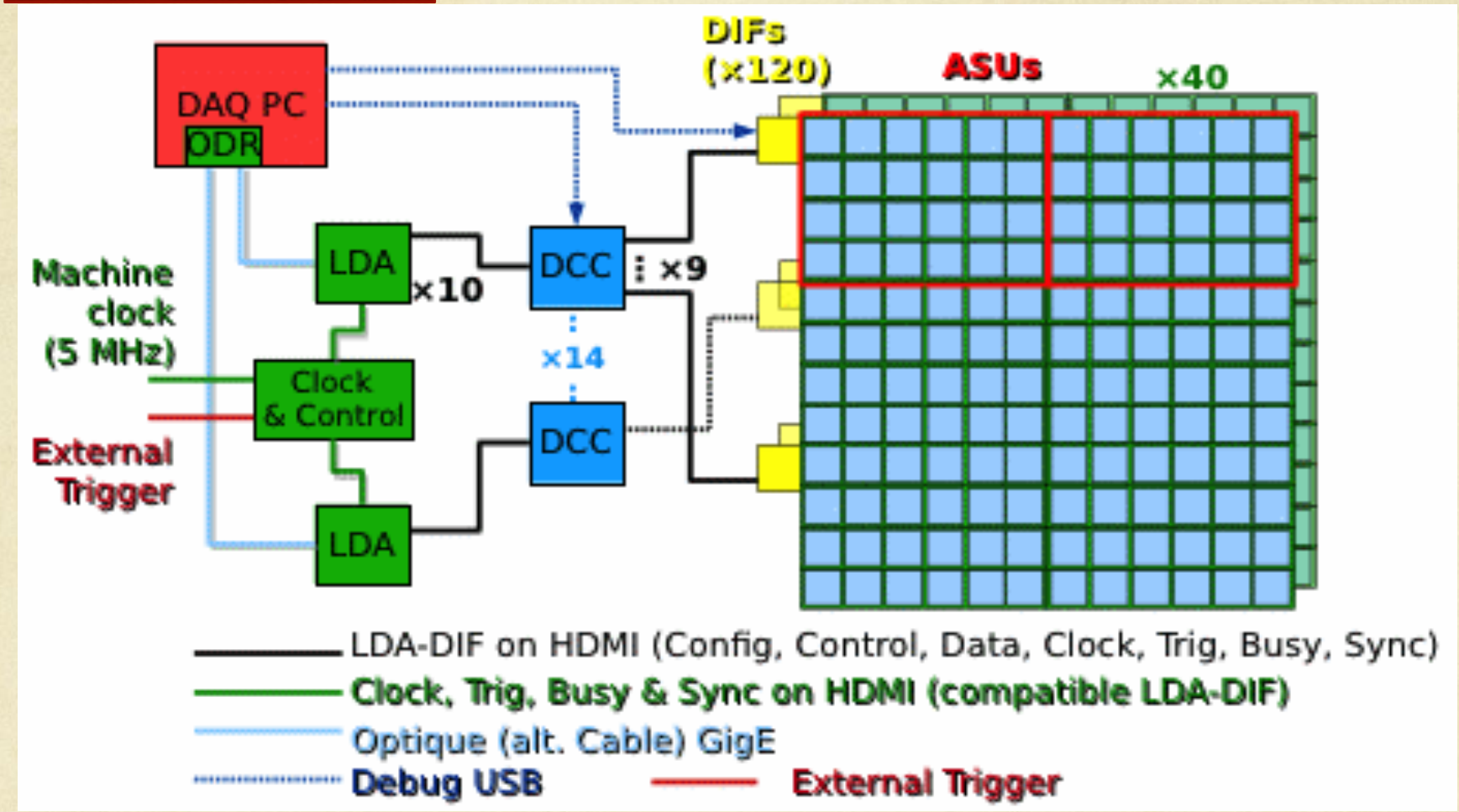
To be packaged in a TQFP208

Submitted at the end of Feb 2013 (SiGe 0.35µm)

Currently tested.



Acquisition system



This scheme failed and was replaced by a hybrid one using both the DCC(fast commands, synchronization, ramful) and USB(data collection).