R&D Activities at IN2P3 for a Vertex Detector suited to ILC

M. Winter (PICSEL group of IPHC-Strasbourg)

- Sensor design : contrib. from Y.Degerli (AIDA/Saclay) -

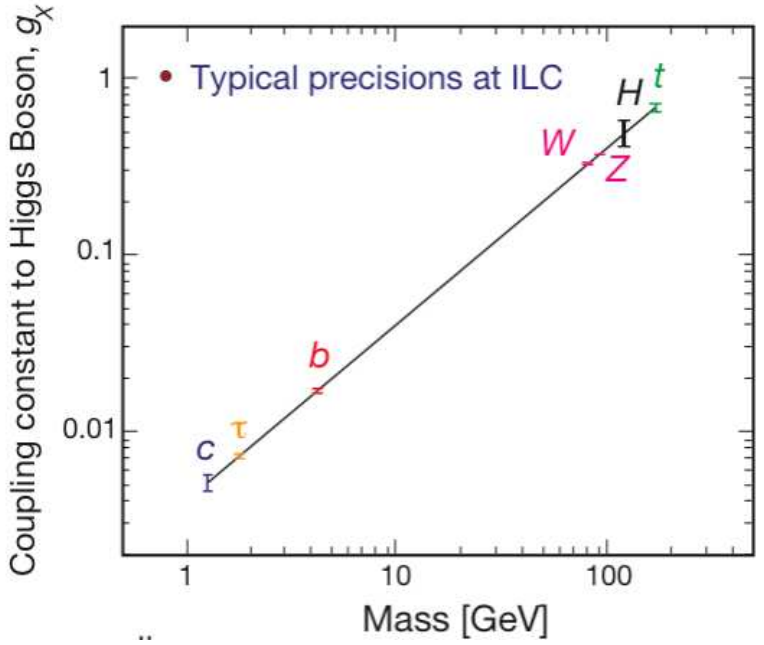
Outline

- *Requirements and topics addressed*
- *Status of CPS development for running at* $\sqrt{s} \lesssim$ *500 GeV* (0.35 μm process)
- *Improvements coming from 0.18* μm *CMOS process*

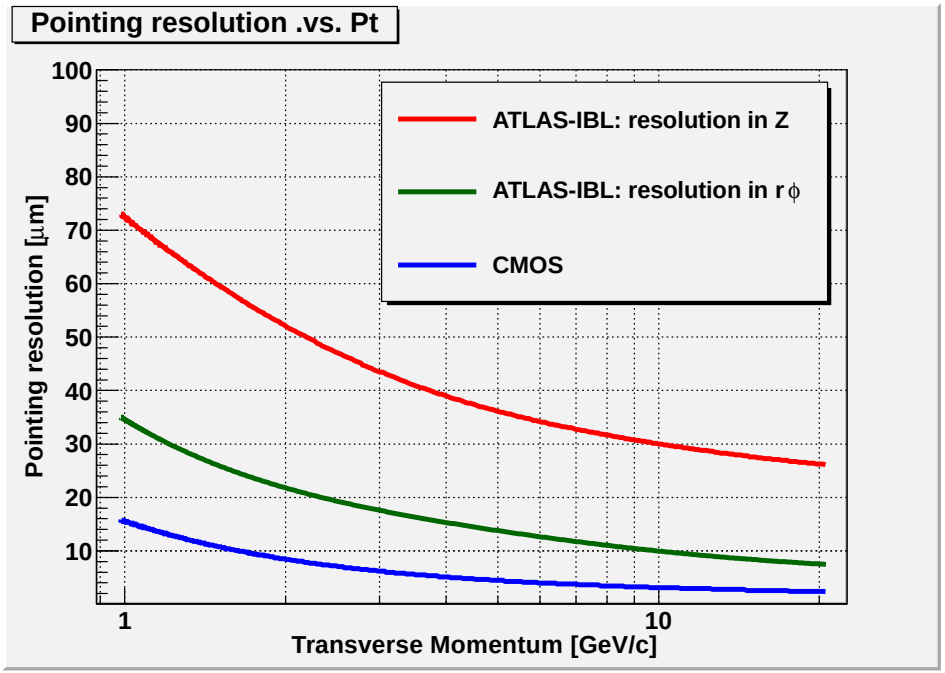
  $\hookrightarrow$ *fast CMOS sensor (AROM) with* μs *level timestamping*
- *Outcome of a 0.18* μm *CMOS technology characterisation*
- *Plans for the coming years*
- *Ladder developments*
- *Summary*

ILC Vertexing Performance Goals

- CMOS PIXEL SENSORS **(CPS) pioneering devt triggered by ILC vertex detector requirements :**
  - ⁕ unprecedented granularity & material budget (very low power)
  - ⁕ much less demanding running conditions than at LHC
    - ⇛ alleviated read-out speed & radiation tolerance requests
  - ⁕ ILC duty cycle ∼ 1/200
    - ⇛ power saving by power pulsing sub-systems



- **Vertexing goal:**
  - ⁕ achieve high efficiency & purity flavour tagging
    - ⟼ charm & tau, jet-flavour !!!
  - ↪ $\sigma_{R\phi,Z} \leq 5 \oplus 10/p \cdot sin^{3/2}\theta \ \ \mu m$
    - ▷ LHC: $\sigma_{R\phi} \simeq 12 \oplus 70/p \cdot sin^{3/2}\theta$
  - ▷ Comparison: $\sigma_{R\phi,Z}$(ILD) with VXD made of ATLAS-IBL or ILD-VXD pixels ⟼



The Central Conflict of Vertexing

- A COMPLEX SET OF STRONGLY CORRELATED ISSUES :

  ⁕ **Charged particle sensor technology :**

  highly granular, thin, low power, swift pixel sensors

  ⁕ **Micro-electronics :**

  highly integrated, low power, SEE safe, r.o. μcircuits

  ⁕ **Electronics :**

  high data transfer bandwith (no trigger), some SEE tol.

  low mass power delivery, allowing for power cycling

  ⁕ **Mechanics :**

  rigid, ultra-light, heat but not electrical conductive,
  mechanical supports, possibly with $C_{\Delta t} \simeq C^{Si}_{\Delta t}$

  very low mass, preferably air, cooling system

  micron level alignment capability

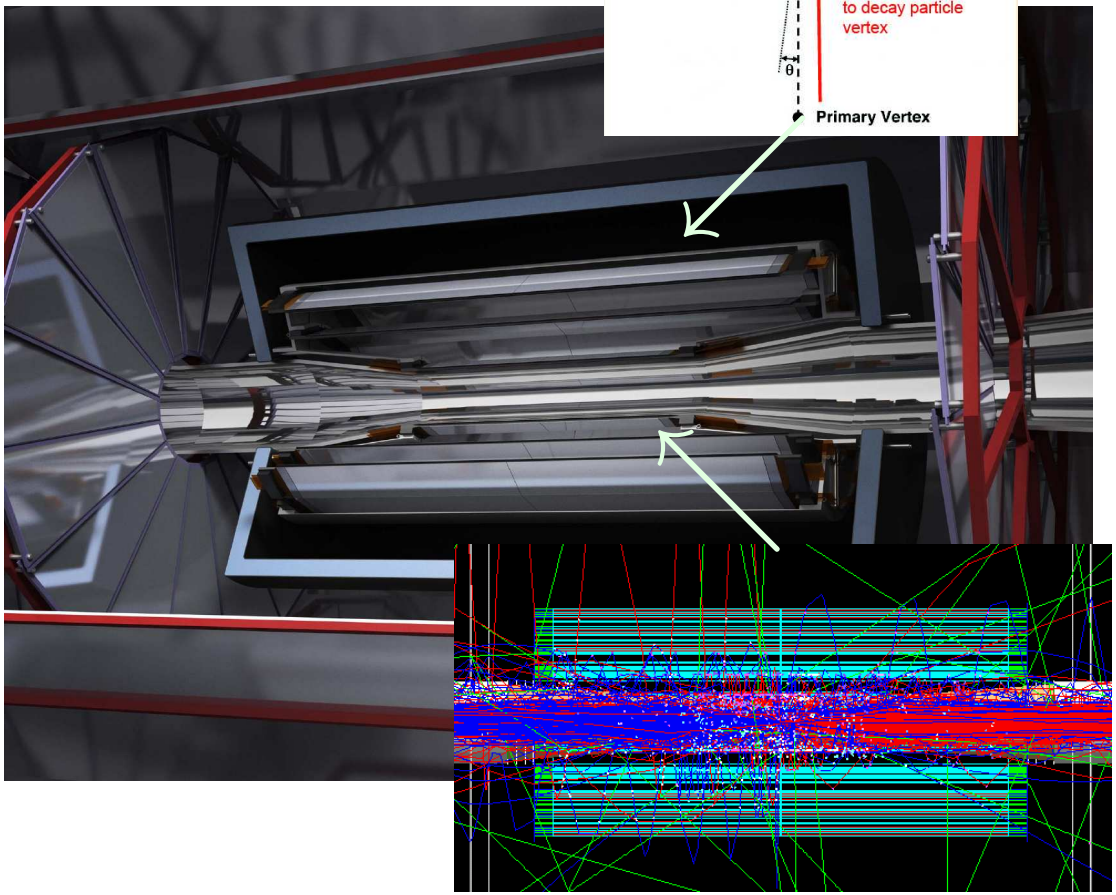
  ⁕ **EM compliance :**

  power cycling in high B field $\Rightarrow$ F(Lorentz)

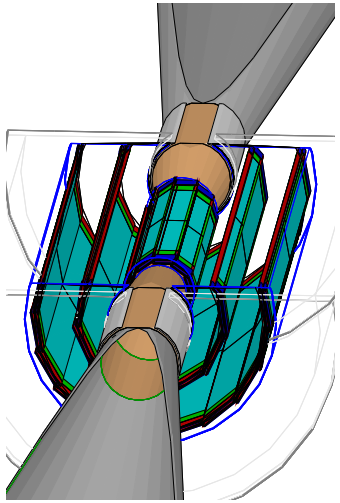
  higher mode beam wakefield disturbance $\Rightarrow$ pick-up noise ?

  ⁕ **Radiation load and SEE compliance at T_{room}**

  $\Rightarrow$ reduced material budget

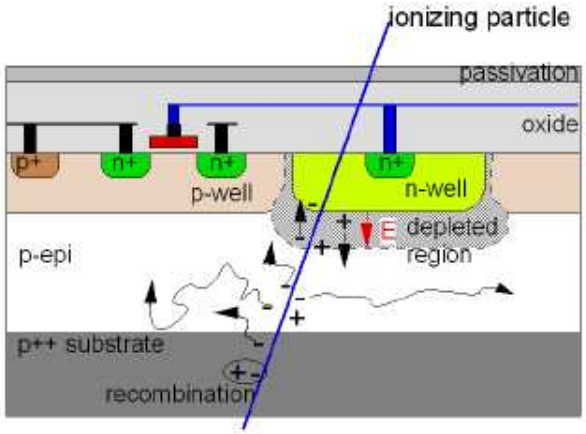


Topics Addressed by the R&D

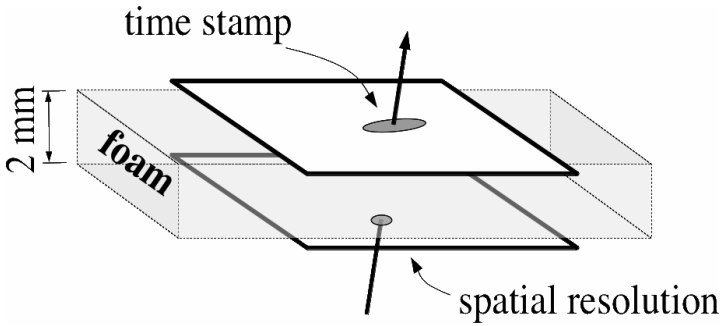


- VERTEX DETECTOR CONCEPT :
  - Cylindrical geometry based on 3 concentric 2-sided layers
  - Layers equipped with 3 different CMOS Pixel Sensors (CPS)

- PIXEL SENSOR DEVELOPMENT:
  - Exploit CPS potential & IPHC expertise
  - R&D performed in synergy with other applications
    ↪ EUDET-BT, STAR, ALICE, CBM, ...
  - CPS ≡ unique technology being simultaneously
    granular, thin, integrating full FEE, industrial & cheap
  - Address trade-off btw spatial resolution & read-out speed



- DOUBLE-SIDED LADDER DEVELOPMENT:
  - Develop concept of 2-sided ladder using 50 μm thin CPS
  - Develop concept of mini-vectors providing
    high spatial resolution & time stamping
  - Address the issue of high precision alignment
    & power cycling in high magnetic field

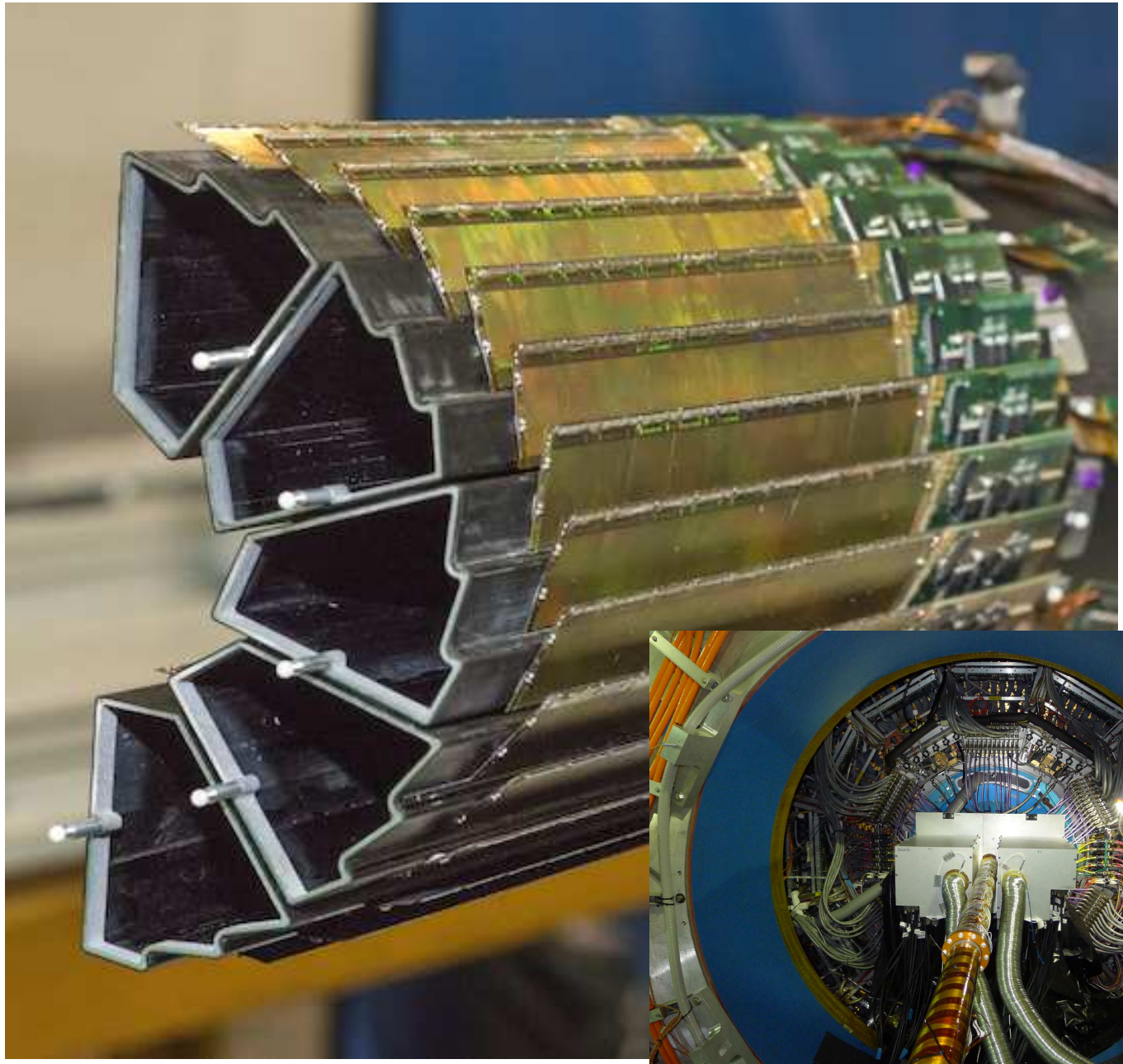


DEVELOPMENT OF CMOS SENSORS

STAR-PXL

HALF-BARREL :

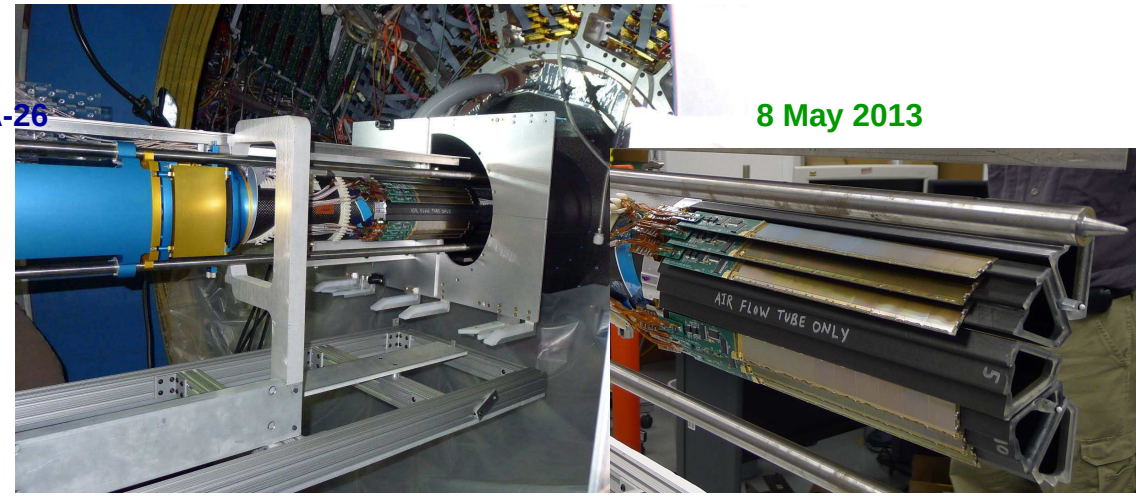
- **20 ladders (0.37% X_0)**
- **200 sensors**
- **$180 \cdot 10^6$ pixels**
- **air flow cooling :**
  $T \lesssim 35^\circ C$
- **$\sigma_{sp} < 4\ \mu m$**
- **rad. load $\gg$ ILC values**
- **$t_{r.o.} \simeq 190\ \mu s$**
  $\hookrightarrow$ **ILC : O(10) μs !**



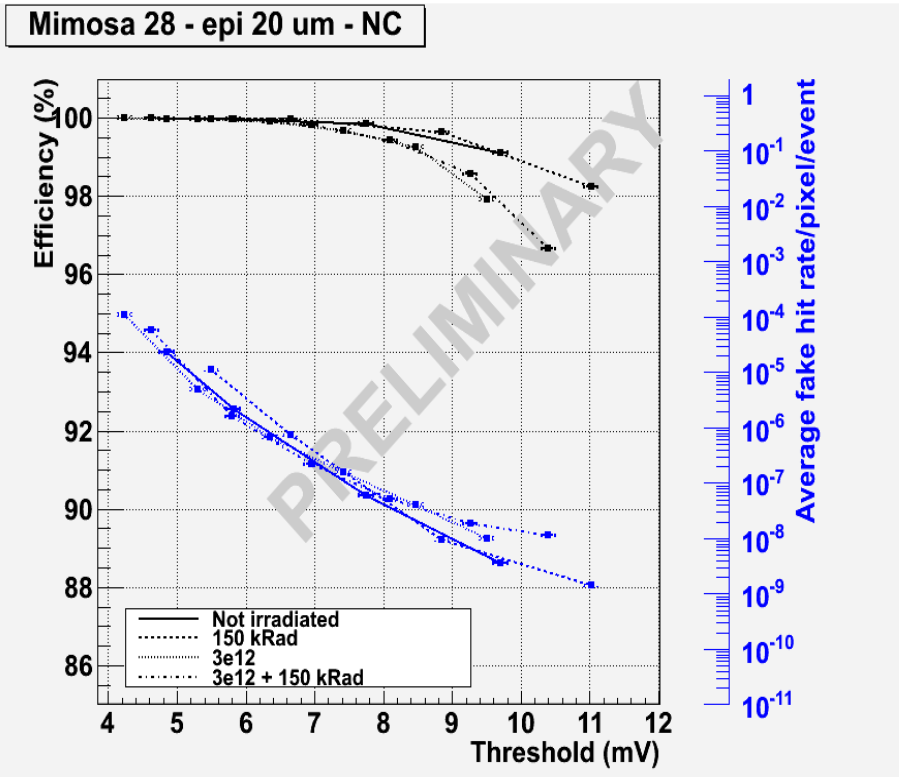
Installed in January 2014

State-of-the-Art: MIMOSA-28 for the STAR-PXL

- Main characteristics of ULTIMATE ($\equiv$ MIMOSA-28):
  - ⁕ rolling shutter read-out derived from EUDET BT chip: MIMOSA-26
  - ⁕ 0.35 μm process with high-resistivity epitaxial layer
  - ⁕ column // architecture with in-pixel cDS & amplification
  - ⁕ end-of-column discrimination & binary charge encoding
  - ⁕ on-chip zero-suppression
  - ⁕ active area: 960 colums of 928 pixels (19.9$\times$19.2 mm^2)
  - ⁕ pitch: 20.7 $\mu m \longmapsto \sim$ 0.9 million pixels
    $\hookrightarrow$ charge sharing $\Rrightarrow$ $\sigma_{sp} \gtrsim$ 3.5 μm
  - ⁕ JTAG programmable
  - ⁕ t$_{r.o.} \lesssim$ 200 μs ($\sim$ 5$\times$10^3 frames/s) $\Rrightarrow$ suited to $>$10^6 part./cm^2/s
  - ⁕ 2 outputs at 160 MHz
  - ⁕ $\sim$ 150 mW/cm^2 power consumption
  - ⁕ N $\lesssim$ 15 e$^-$ ENC at 30-35°C
  - ⁕ ϵ_{det} versus fake hit rate $\longmapsto$ $\longmapsto$ $\longmapsto$ $\longmapsto$
  - ⁕ Radiation tolerance : 3$\cdot$10^{12} n$_{eq}$/cm^2 & 150 kRad at 30-35°C
  - ⁕ Detector construction under way (40 ladders made of 10 sensors)



8 May 2013



▷▷▷ 1st step: Commissioning of 3/10 of detector completed at RHIC with pp collisions in May-June 2013

▷▷▷ next step: Start of physics with full detector in Feb. 2014

CMOS Pixel Sensors for the ILD-VXD (1/3)

- **Two types of CMOS Pixel Sensors :**
  - ⁂ **Inner layers** ($\lesssim$ 300 cm^2) :

    Priority to read-out speed & spatial resolution

    ↪ small pixels (16×16 / 80 μm^2)

    with binary charge encoding

    ↪ $t_{r.o.} \sim$ 50 / 10 μs; $\sigma_{sp} \lesssim$ 3 / 6 μm

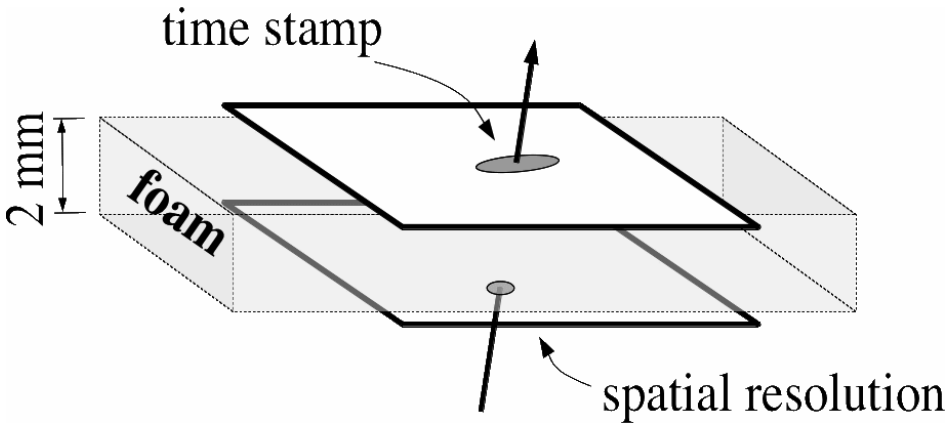
  - ⁂ **Outer layers** ($\sim$ 3000 cm^2) :

    Priority to power consumption and good resolution

    ↪ large pixels (35×35 μm^2)

    with 3-4 bits charge encoding

    ↪ $t_{r.o.} \sim$ 100 μs; $\sigma_{sp} \lesssim$ 4 μm



⁂ Total VXD instantaneous/average power $<$ 600/12 W (0.18 μm process)

- **2-sided ladder concept for inner layer :**

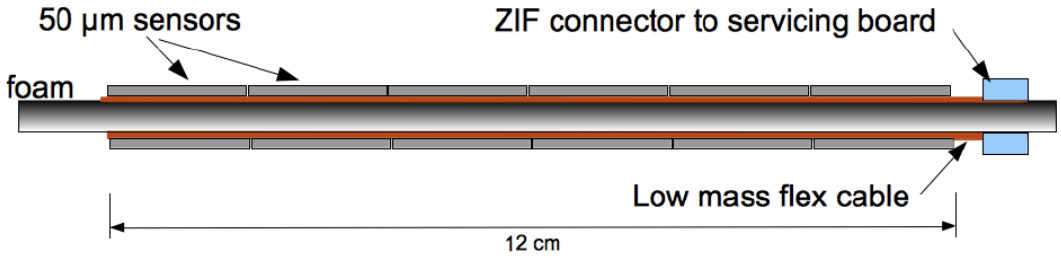
  ↪ PLUME collaboration

  - ⁂ **Square pixels** (16×16 μm^2)

    on internal ladder face ($\sigma_{sp} < 3\ \mu m$)

  - ⁂ **Elongated pixels** (16×64/80 μm^2)

    on external ladder face ($t_{r.o.} \sim 10\ \mu s$)



CMOS Pixel Sensors for the ILD-VXD (2/3)

- **From the STAR-PXL to the ILC-VXD :**

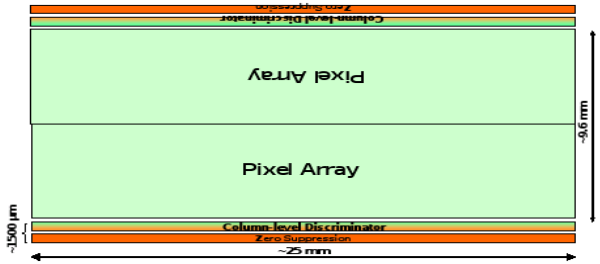
Detector	σ_{sp}	t_{int}	**Dose** (30°C)	**Fluence** (30°C)
STAR-PXL	$\gtrsim$ 3.5 μm	190 μs	150 kRad	3·10^{12}n$_{eq}$/cm^2
ILD-VXD/In	$<$ 3 μm	50/10 μs	$<$ 100 kRad	$\lesssim$ 10^{11}n$_{eq}$/cm^2
ILD-VXD/Out	$\lesssim$ 4 μm	100 μs	$<$ 10 kRad	$\lesssim$ 10^{10}n$_{eq}$/cm^2

- **Final "500 GeV" CPS prototypes :** fab. in Winter 2011/12 **(0.35 μm process for economic reasons)**

  ✳ **MIMOSA-30:** inner layer prototype with 2-sided read-out ▷ ▷ ▷

  ↪ one side : 256 pixels (16×16 μm^2)

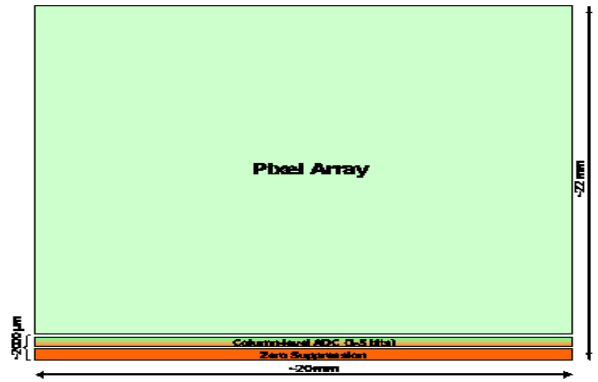
  other side : 64 pixels (16×64 μm^2)



  ✳ **MIMOSA-31:** outer layer prototype ▷ ▷ ▷

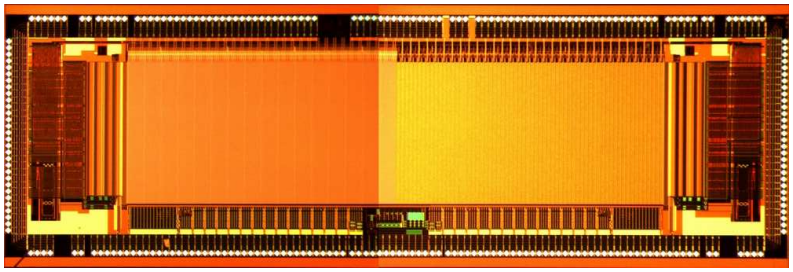
  ↪ 48 col. of 64 pixels (35×35 μm^2)

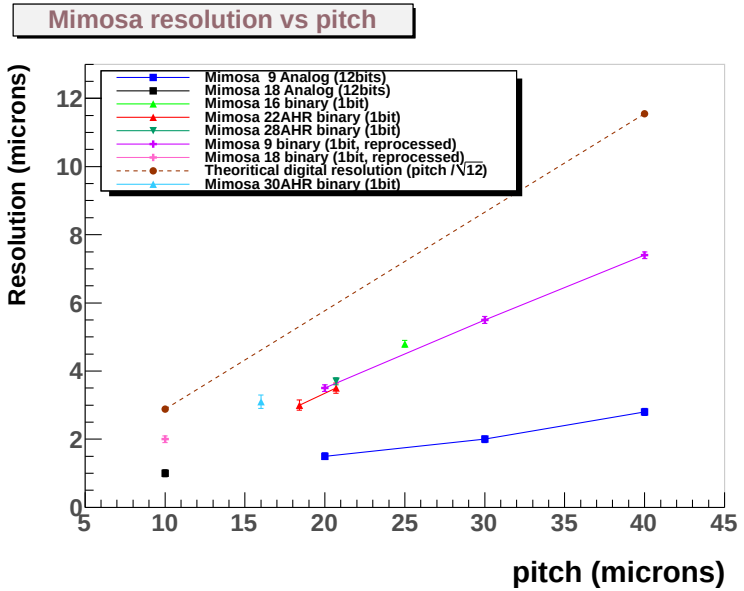
  ended with 4-bit ADC



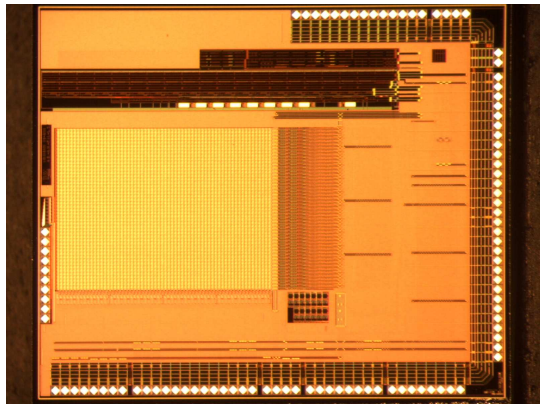
CMOS Pixel Sensors for the ILD-VXD (3/3)

- **MIMOSA-30: prototype for ILD-VXD innermost layer** ▷ ▷ ▷
  - ⁂ 0.35 CMOS μm process with high-resistivity epitaxy
  - ⁂ in-pixel CDS, rolling shutter read-out, binary sparsified output
  - ⁂ columns length $\simeq$ final sensor (4-5 mm long)
  - ⁂ **high resolution side : pixels of 16$\times$16 μm^2 $\Rrightarrow$ expect $\sigma_{sp} < 3\ \mu m$**
    - 128 columns (discri) & 8 col. (analog) of 256 rows
    - read-out time $\lesssim 50\ \mu s$
  - ⁂ **time stamping side : pixels of 16$\times$64 μm^2 $\Rrightarrow$ $t_{r.o.} \sim$ 10 μs**
    - (expect $\sigma_{sp} \sim 6\ \mu m$)
    - 128 columns (discri) and 8 col. (analog) of 64 rows
    - lab tests positive : N $\sim$ 15 e$^-$ ENC & discri. all OK for $t_{r.o.} = 10\ \mu s$
  - ⁂ beam tests (CERN-SPS) in July '12 $\Rrightarrow$ σ_{sp} ▷ ▷ ▷





- **MIMOSA-31: prototype for ILD-VXD outer layers**
  - ⁂ pixels of 35$\times$35 μm^2 (power saving) ▷ ▷ ▷
  - ⁂ 48 columns of 64 pixels ended with 4-bit ADC (1/10 of full scale chip)
    $\hookrightarrow$ expect $\sigma_{sp} \lesssim 3.5\ \mu m$
  - ⁂ $t_{r.o.} \sim 10\ \mu s$ (1/10 of full scale chip $\rightarrowtail$ $\sim 100\ \mu s$)



Acceleration of Frame Read-Out

- **Motivations for faster read-out:**
  - ⁕ robustness w.r.t. predicted 500 GeV BG rate (keep inner radius small, ...)
  - ⁕ standalone inner tracking capability (e.g. soft tracks)
  - ⁕ compatibility with high-energy running: expected beam BG at $\sqrt{s} \gtrsim 1$ TeV $\simeq$ 3–5$\times$BG (500 GeV)

- **How to accelerate the elongated pixel read-out**
  - ⁕ elongated pixel dimensions allow for in-pixel discri. $\Rrightarrow$ $\geq$ 2 faster r.o.
  - ⁕ read out simultaneously 2 or 4 rows $\Rrightarrow$ 2-4 faster r.o./side
  - ⁕ subdivide pixel area in 4-8 sub-arrays read out in // $\Rrightarrow$ 2-4 faster r.o./side
  - ▷ 0.18 μm process needed: 6-7 ML, design compactness, in-pixel CMOS T, ...
  - ⁕ conservative step: 2 discri./col. **end** (22 μm wide) $\Rrightarrow$ simult. 2 row r.o.

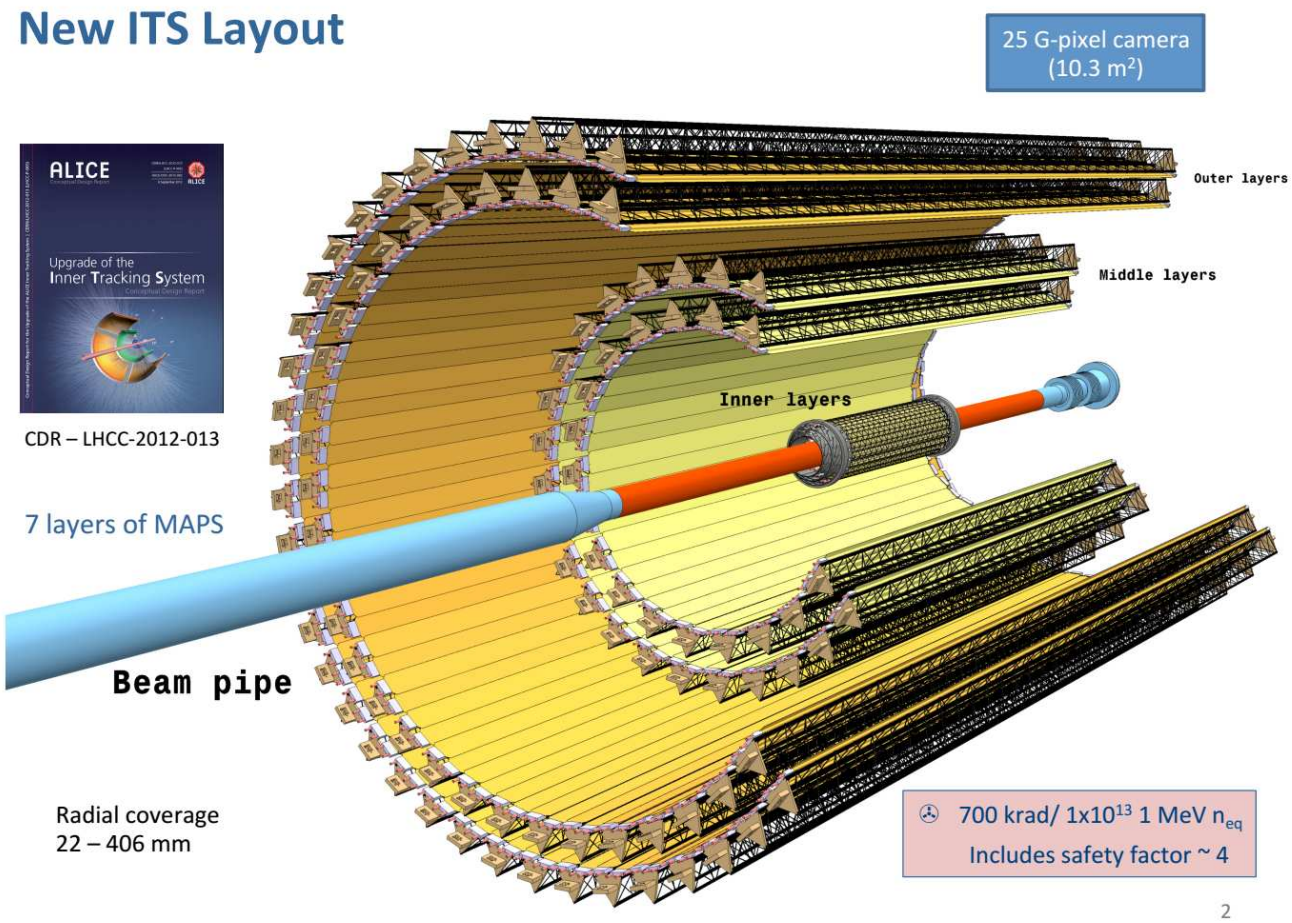
- **Expected VXD performances at 1 TeV (and 0.5 TeV)**

Layer	σ_{sp} MIMOSA/AROM	t_{int} MIMOSA/AROM	**Occupancy [%]** 1 TeV (0.5 TeV)	**Power** inst./average
VXD-1	3 / 5-6 μm	50 / 2 μs (10 μs)	4.5(0.9) / 0.5(0.1)	250/5 W
VXD-2	4 / 10 μm	100 / 7 μs (100 μs)	1.5(0.3) / 0.2(0.04)	120/2.4 W
VXD-3	4 / 10 μm	100 / 7 μs (100 μs)	0.3(0.06) / 0.05(0.01)	200/4 W

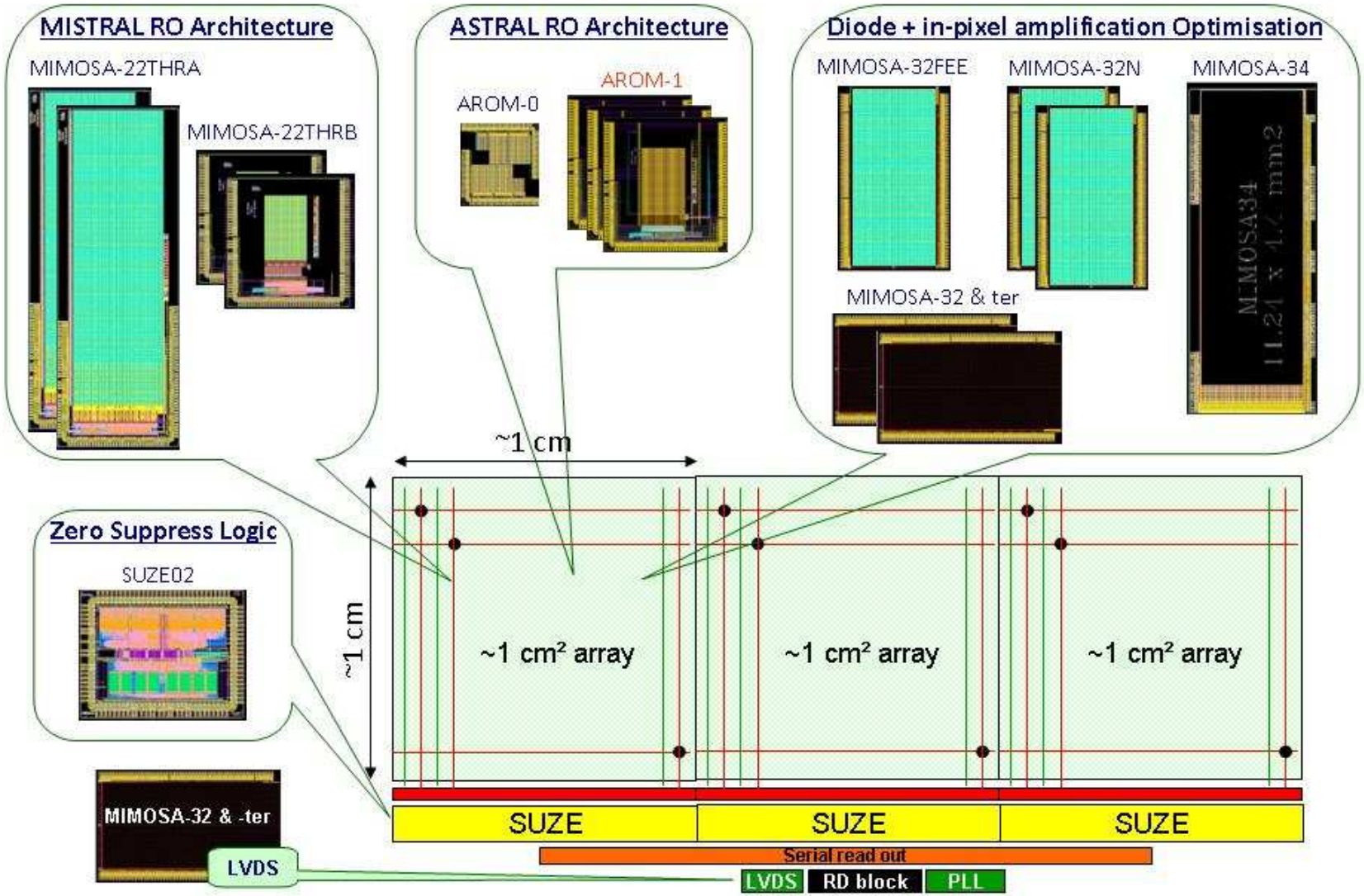
ALICE-ITS Upgrade

- 2 alternative sensors developped :
  - ⁕ Baseline : **ASTRAL** (in-pixel discri.)
    - ↪ $\gtrsim$ 15 μs, 85 mW/cm^2
  - ⁕ Back-up : **MISTRAL** (end-of-col. discri.)
    - ↪ $\gtrsim$ 30 μs, $<$ 200 mW/cm^2

- All main components validated in 2013 :
  - ⁕ sensing node properties
  - ⁕ in-pixel ampli+CDS
  - ⁕ in-pixel discriminators
  - ⁕ rolling-shutter with end-of-col. discri.
  - ⁕ simultaneous 2-row read-out
  - ⁕ sparse data scan
  - ⁕ programmable chip steering (JTAG)
    - ↪ **outcome integrated in ITS-TDR**



CPS fabricated in 2012/13 in 0.18 μm Process



SNR of Pixel Array

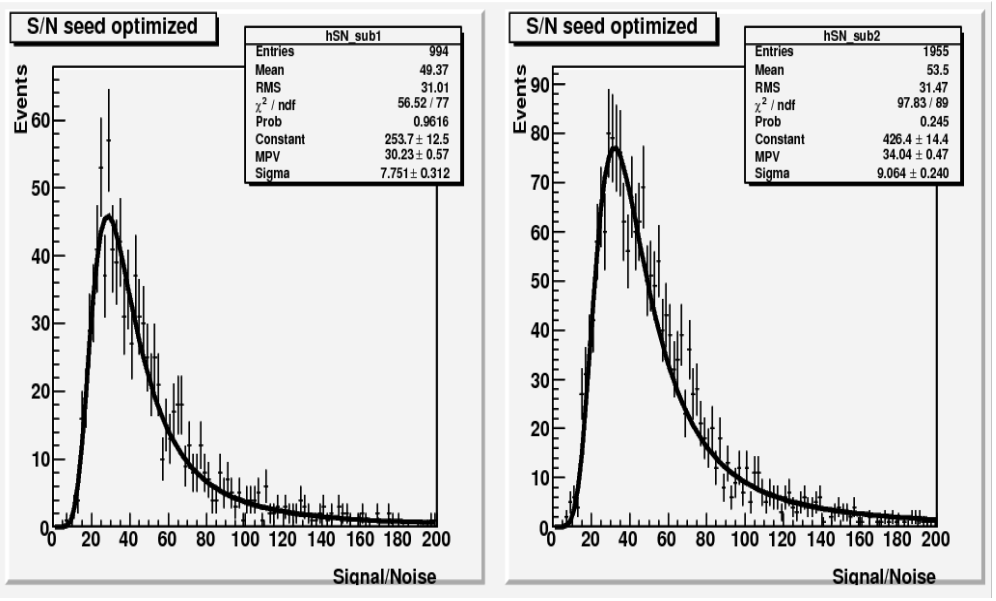
- MIMOSA-22THRa1 exposed to $\sim$ 4.4 GeV electrons (DESY) in August 2013
- Analog outputs of 8 test columns (no discri.)

  $\hookrightarrow$ SNR with HR-18 epitaxy, at T=30°C

  ⁂ Noise determination with beamless data taking

  ⁂ Ex: S2 (T gate L/W=0.36/1 μm against RTS noise)

  S1 (T gate L/W=0.36/2 μm against RTS noise)



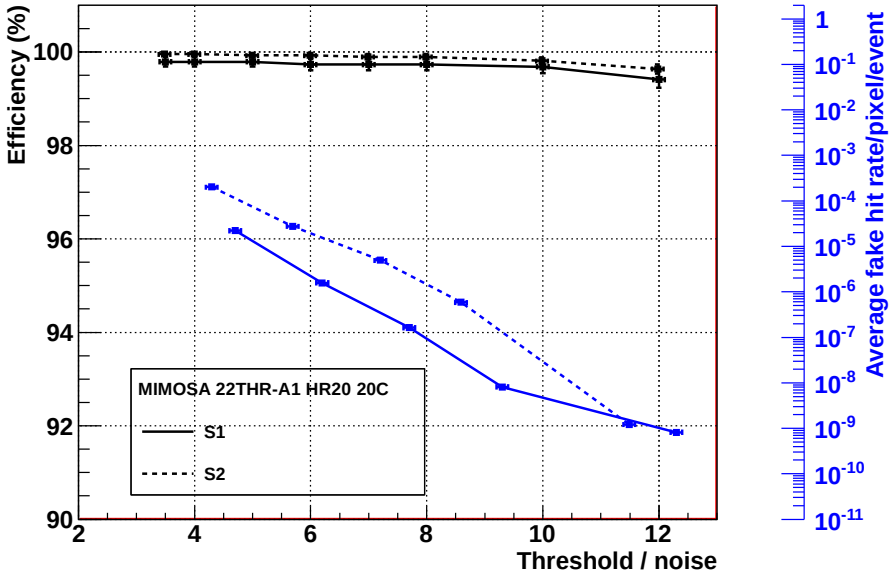
- Results :

  ⁂ Charge collected in seed pixel $\simeq$ 550 e$^-$

  ⁂ Detection efficiency of S1 & S2 $\gtrsim$ 99.5%
  while Fake rate $\lesssim$ O(10^{-5}) for
  Discrimination Thresholds in range $\sim$ 5N $\longmapsto$ $>$ 10N

  ⁂ Mitigation of Fake Hits due to RTS
  noise fluctuations confirmed

  ⁂ A few 10^{-3} residual inefficiency may come
  from BT-chip association missmatches
  and non-optimised cluster algorithme

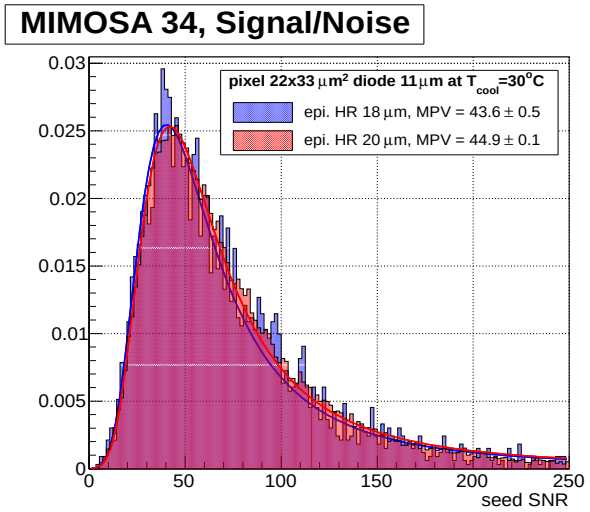


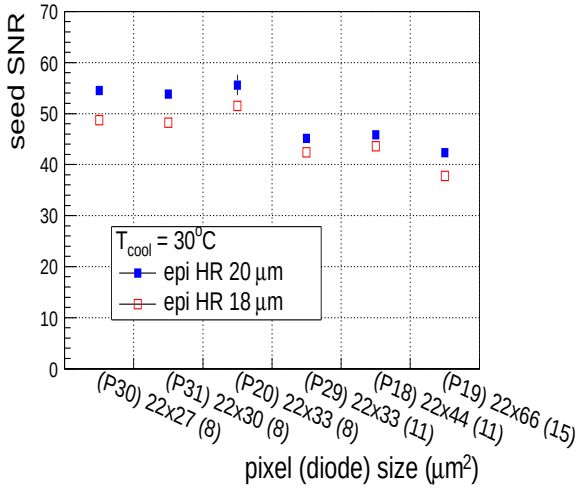
Pixel Optimisation : Epitaxial Layer and Sensing Node

- **Pixel charge coll. perfo. for HR-18 & VHR-20 (no in-pixel CDS) :**
  - ⁕ SNR distributions ⟼ MPV & low values tail
  - ⁕ 22×33 μm^2 (2T) pixels at 30°C

⇛ **Results :**

- ◇ only ∼ 0.1 % of cluster seeds exhibit SNR $\lesssim$ 7–8
- ◇ SNR(VHR-20) ∼ 5-10% higher than SNR(HR-18)

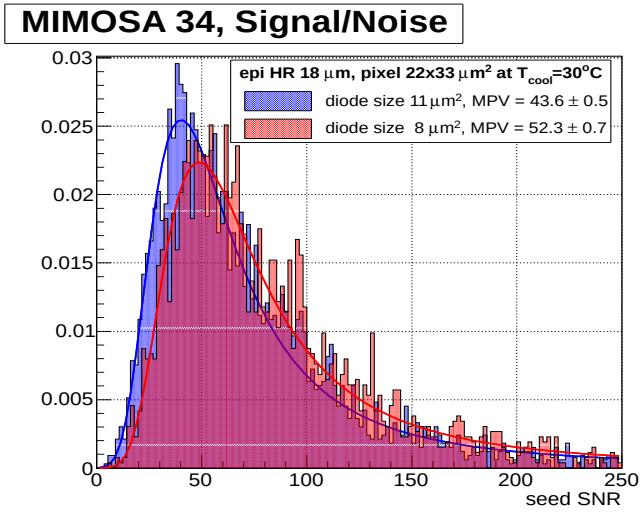


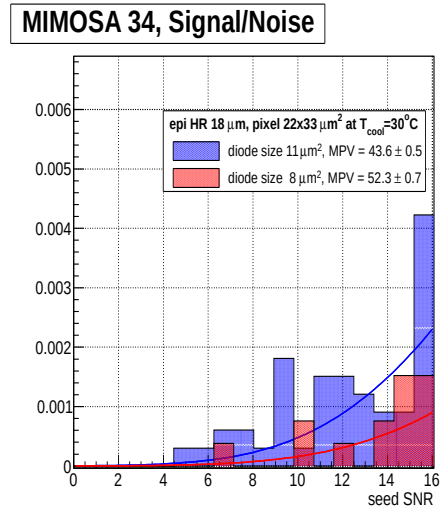


- **Pixel charge coll. perfo. for 2 diff. sensing nodes:**
  - ⁕ 10.9 μm^2 large sensing diode
  - ⁕ 8 μm^2 cross-section sensing diode underneath 10.9 μm^2 large footprint

⇛ **Results :**

- ◇ 8 μm^2 diode features nearly 20% higher SNR(MPV) & much less pixels at small SNR (e.g. SNR <10)
  ⟼ Q_{clus} ≃ 1350/1500 e^- for 8/10.9 μm^2
  ⇛ marginal charge loss with 8 μm^2 diode
- ◇ radiation tolerance to 250 kRad & 2.5·10^{12} n_{eq}/cm^2 at 30°C OK





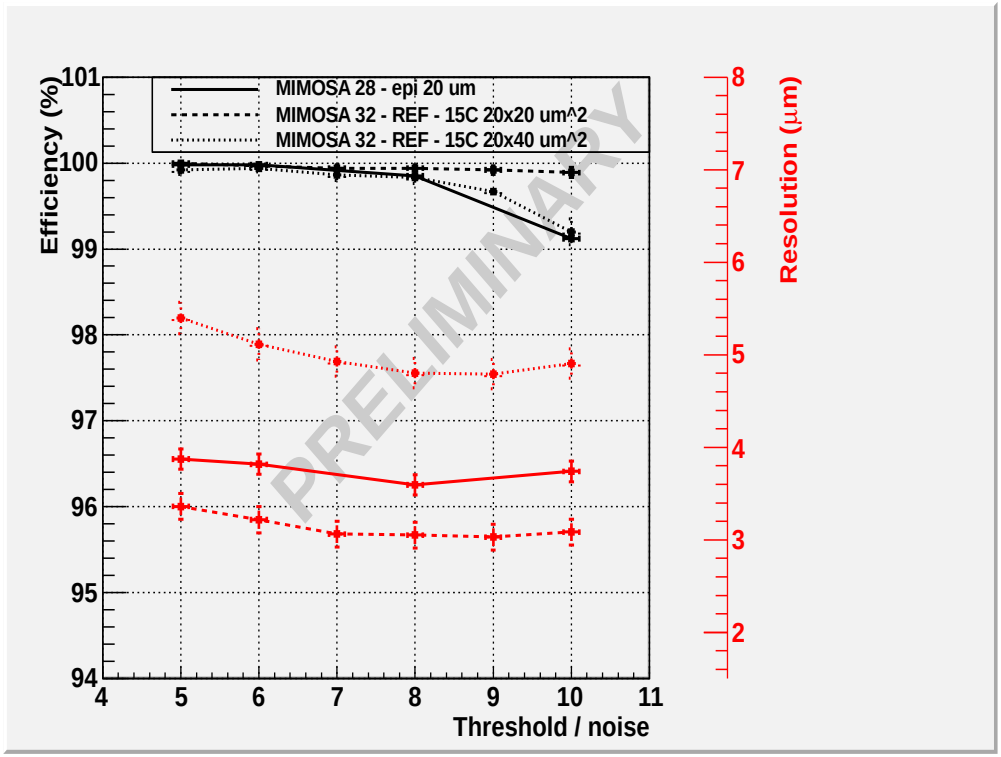
Spatial Resolution

- **Beam test (analog) data used to simulate binary charge encoding :**

  ✳ Apply common SNR cut on all pixels using <N>

  ⟶ simulate effect of final sensor discriminators

  ✳ Evaluate single point resolution (charge sharing) and detection efficiency vs *discriminator threshold* for 20x20; 22x33; 20x40; 22x66 μm^2 pixels



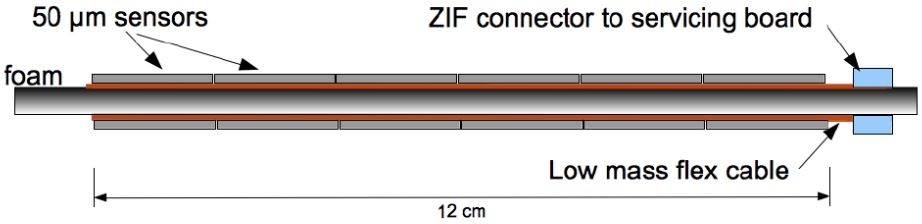
- **Comparison of 0.18 μm technology ($> 1\ k\Omega \cdot cm$) with 0.35 μm technology ($\lesssim 1\ k\Omega \cdot cm$)**

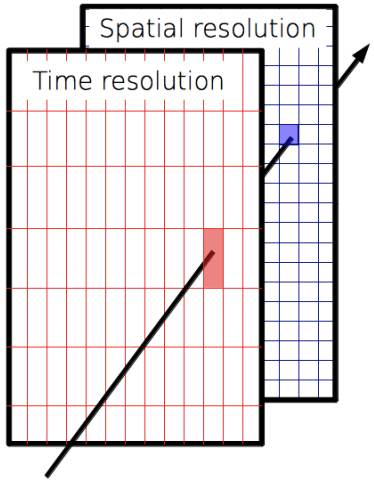
Process ▷	0.35 μm	0.18 μm			
Pixel Dim. [μm^2]	20.7×20.7	20×20	22×33	20×40	22×66
$\sigma_{sp}^{bin}[\mu m]$	3.7 ± 0.1	3.2 ± 0.1	∼ 5	5.4 ± 0.1	∼ 7

DEVELOPMENT OF ULTRA-LIGHT DOUBLE-SIDED LADDERS

Sensor Integration in Ultra Light Devices

- **2-sided ladders with time stamping for the ILD-VXD :**
  - manyfold bonus expected from 2-sided ladders:
    alignment, pointing accuracy (shallow angle),
    compactness, redundancy, etc.
  - studied by PLUME coll. (Bristol, DESY, IPHC) & AIDA (EU)
    ↪ **P**ixelated **L**adder using **U**ltra-light **M**aterial **E**mbedding
  - square pixels for single point resolution on beam side
  - elongated pixels for 5-50 times shorter r.o. time on other side
  - correlate hits generated by traversing particles
  - expected total material budget $\sim$ 0.3 % X_0

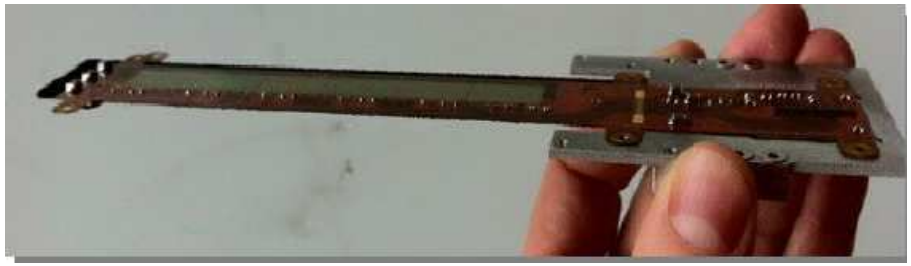


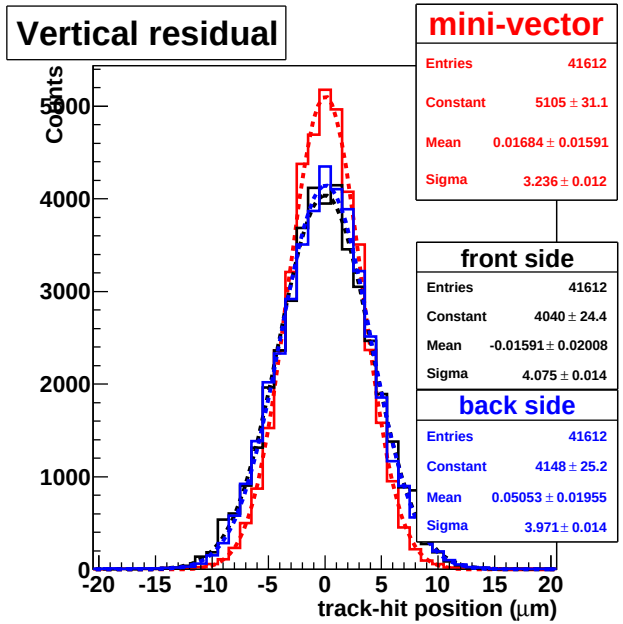


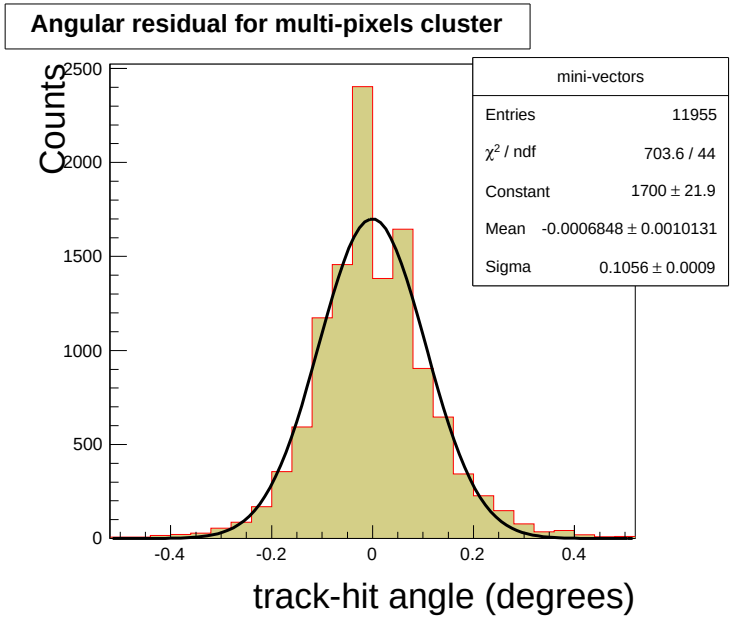
- **Prototypes fabricated :**
  - based on 2×6 MIMOSA-26 sensors mounted on each ladder face
  - mechanical support : 2 mm thick low density SiC foam
  - total material budget $\sim$ 0.6 % X_0
  - beam tests at CERN-SPS (traversing m.i.p.) in Nov. ’11

2-Sided Ladder Beam Test Results

- **PLUME prototype-2010 tested at SPS in Nov. 2011:**
  - *Beam telescope : 2 arms, each composed of 2 MIMOSA-26 sensors*
  - *DUT : 1 PLUME ladder prototype (0.6 % X_0)*
    - ↪ *6 MIMOSA-26 sensors on each ladder face ($>$ 8 Mpixels)*
  - *CERN-SPS beam : $\gtrsim$ 100 GeV "π^-" beam*
  - *BT (track extrapolation) resolution on DUT $\sim$ 1.8 μm*
  - *Studies with PLUME perpendicular and inclined ($\sim 36^\circ$) w.r.t. beam line*
  - *Preliminary results (no pick-up observed): combined impact resolution & pointing resolution*







- **New PLUME proto. under construction with 0.35 % X_0** (X-sect.) $\longmapsto$ **beam tests in Q4/2014** (SPS ?)

CMOS Pixel Sensors (CPS): A Long Term R&D

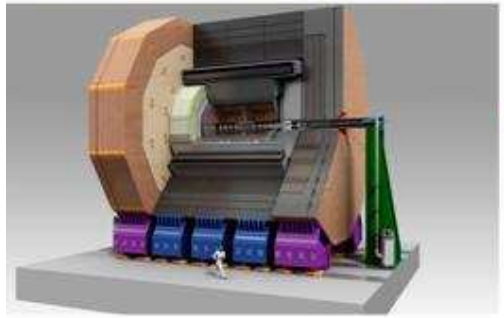
- ***Initial objective: ILC, with staged performances***
  - *CPS applied to other experiments with intermediate requirements*

EUDET 2006/2010

Beam Telescope

ILC >2020

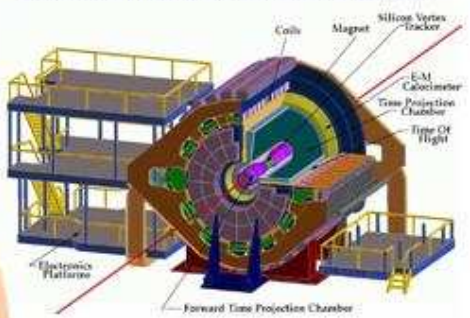
International Linear Collider



EUDET (R&D for ILC, EU project)
STAR (Heavy Ion physics)
CBM (Heavy Ion physics)
ILC (Particle physics)
HadronPhysics2 (generic R&D, EU project)
AIDA (generic R&D, EU project)
FIRST (Hadron therapy)
ALICE/LHC (Heavy Ion physics)
EIC (Hadron physics)
CLIC (Particle physics)
BESIII (Particle physics)
...

STAR 2013

Solenoidal Tracker at RHIC

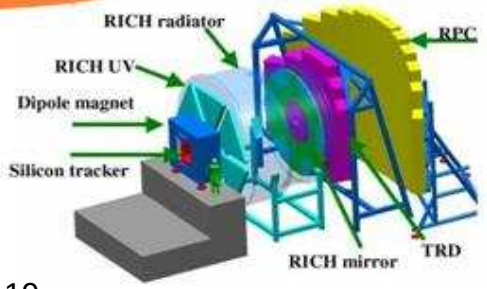


ALICE 2018

A Large Ion Collider Experiment

CBM >2018

Compressed Baryonic Matter



Plans for the Upcoming Years

- R&D PLANS ON CPS :
  - realise full scale sensor in 0.18 μm techno. : ASTRAL ($\lesssim$ 20 μs) & MISTRAL ($\gtrsim$ 30 μs)
  - achieve O(1) μs time stamping with elongated pixels $\Rrightarrow$ bunch tagging
  - validate concept with 3-bit charge encoding ADC in 0.18 μm techno.
  - study alternative approach using Fine Pixel CPS (4-5 μm pitch)
- R&D OF 2-SIDED LADDERS :
  - validate ladder design resulting in 0.35 % X_0 material budget
  - validate ladder concept based on fast/precise sensors on 1st/2nd face (e.g. ASTRAL & MIMOSA-26)
  - validate power pulsing in high magnetic field
  - investigate 2-sided ladder design allowing for $<$ 0.3 % X_0
- FRAMEWORK : R&D CONTINUATION UNTIL EARLY 2020S
  - ALICE-ITS until 2016
  - CBM-MVD until 2018
  - MIMOSA-26/-28 users : EUDET-BT, FIRST, EIC, NA-61, NA-63, BES-III, biomedical & X-Ray -imaging, dosimetry, hadrontherapy, ...
  - H2020, LIA, ...

Plans for the Upcoming Years

- 2014 :
  - Sensors : realise & validate full scale architectures for ALICE-ITS (ASTRAL ans MISTRAL)
  - Ladders : realise and test 0.35 % X_0 2-sided ladder based on MIMOSA-26
- 2015 :
  - Sensors : realise final prototype for the ALICE-ITS
  - Ladders : test of vertex detector "sector" $\equiv$ 3 consecutive pairs of ladders on beam
- 2016 :
  - Sensors : production tests of ALICE-ITS sensors $\rightarrowtail$ evolution towards CBM-MVD/FAIR (ASTRAL)
  - Ladders : realise 2-sided ladder equipped with 2 different chips (e.g. ASTRAL / MIMOSA-26)
- 2017 :
  - Sensors : follow ITS production, production of sensors for CBM-MVD (FAIR)
  - Ladders : beam tests of 2-sided ladder equipped with 2 different chips
- 2018 : Start realisation of large sensors dedicated to ILC VXD

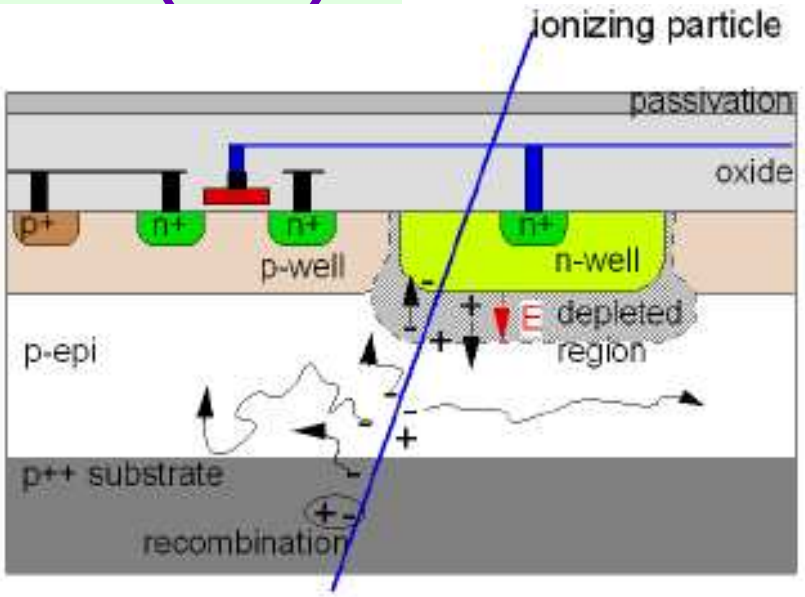
SUMMARY

- R&D ON CPS :
  - Well established architecture achieved and implemented in STAR-PXL (0.35 μm CMOS process)
    $\hookrightarrow$ extendable to sensors suited to ILD-VXD $\lesssim$ 500 GeV
  - Not accessible with 0.35 μm process : standalone tracking, bunch tagging (SiD), 1 TeV running, etc.
    $\hookrightarrow$ 0.18 μm process accessed in 2011 should allow meeting these goals
  - 2012-13 allowed assessing process & realising all major sensor architecture elements
    $\hookrightarrow$ Realisation of complete ASTRAL sensor in 2014 (ITS)
  - Upcoming years : beyond 2014
    - Final ALICE-ITS sensor & CBM-MVD variant (include all main elements for ILD-VXD)
      $\hookrightarrow$ ILC dedicated sensors in 0.18 μm process from 2017/18 on
    - Investigate FPCPS delayed read-out approach

- 2-SIDED LADDERS : PLUME collaboration
  - Prototype based on MIMOSA-26 sensors on the way to achieve 0.35 % X_0
  - Upcoming years : beyond 2014
    - Validate concept of complementary sensors with ASTRAL/MIMOSA-26 & power pulsing in string mag. field
    - Assess added value of double-sided ladders
    - Investigate possibilities to still reduced the ladder material budget $<$ 0.3% X_0

BACK-UP SLIDES

Main Features of CMOS Sensors (CPS)



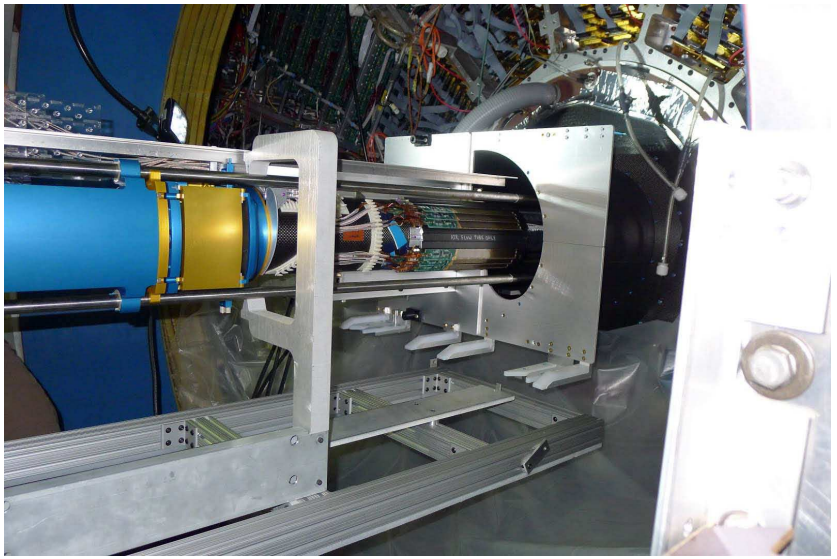
- P-type Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):
    Q $\sim$ 70–80 e-h / $\mu m \mapsto$ signal $\lesssim$ 1000 e^-
    - charge sensing through n-well/p-epi junction
    - excess carriers diffuse and/or drift to diode
      with help of reflection on boundaries
      with p-wells and substrate (high doping)
      $\Rightarrow$ continuous signal sensing (no dead time)

$\triangleright\triangleright\triangleright$ since a few years : high resistivity ($> 1\ k\Omega \cdot cm$) epitaxial layer

- Prominent advantages of CMOS sensors :
  - ◇ **granularity :** pixels of $\lesssim 10 \times 10\ \mu m^2$ $\Rightarrow$ high spatial resolution (e.g. $\lesssim 1\ \mu m$ if needed)
  - ◇ **low material budget :** sensitive volume $\gtrsim$ 10 - 20 μm $\Rightarrow$ total thickness $\lesssim 50\ \mu m$ $\Rightarrow$ thinning $\lesssim 50\ \mu m$
  - ◇ **signal processing μcircuits integrated in the sensors** $\Rightarrow$ compacity, high data throughput, flexibility, etc.
  - ◇ **industrial mass production** $\Rightarrow$ cost, industrial reliability, fabrication duration, multi-project run frequency, technology evolution, ...
  - ◇ **operating conditions :** from $\ll 0^\circ$C to $\gtrsim$ 30-40°C
- Main limitation of the approach : CMOS industry addresses a market far from HEP needs
  - ◇ fab. process parametres not optimised to fully exploit the potential of CPS
  - ◇ **BUT recently accessible processes (epitaxial layer, feature size) have opened up new perspectives**

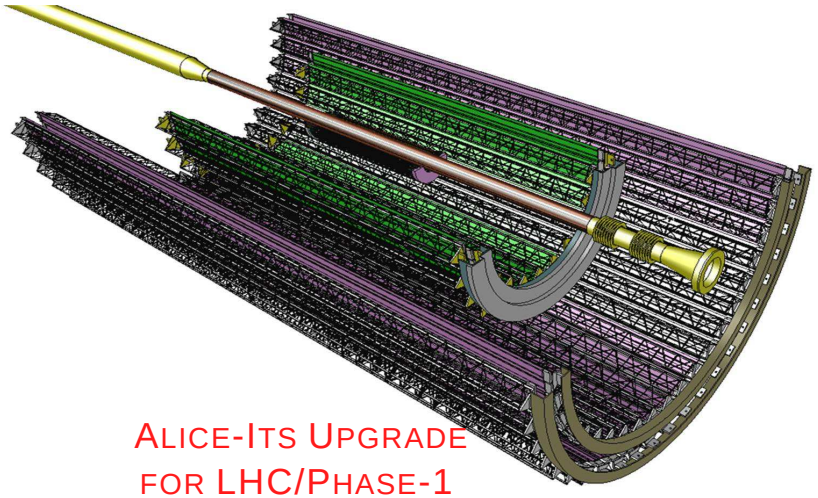
CMOS Pixel Sensors: Present Status

- ESTABLISHED ARCHITECTURE :
  - CMOS process : 0.35 μm, 2-well, 4 ML, 15/20 μm & $\sim$ 1 k$\Omega \cdot cm$ EPI
  - in-pixel CDS
  - end-of column discri. (binary encoding)
  - single-row rolling shutter read-out
  - sparse data scan on chip periphery
  - 18.4/20.7 μm pitch $\Rrightarrow$ $\gtrsim$ 3.3.5 μm resolution
  - used in EUDET BT (115 μs) & STAR-PXL (190 μs)
    - ▷ **recent step:** Commissioning of 3/10 STAR-PXL completed at RHIC with pp & ArAr collisions in May-June 2013



STAR-PXL-3SECT INSERTION
PP & ARAR RUN IN MAY-JUNE'13

- NEW PROCESS UNDER STUDY SINCE 2011/12 :
  - CMOS process : 0.18 μm, 4-well, 6 ML, 15/40 μm & $\sim$ 1-6 k$\Omega \cdot cm$ EPI
  - allows in-pixel discrimination $\Rrightarrow$ faster read-out & reduced power, etc.
  - development driven by ALICE-ITS upgrade & CBM-MVD/FAIR ($\sim$ 20 μs)
    - ▷ **recent step:** Assessment of CMOS proces detection performances & validation of rolling-shutter read-out completed in 2013



ALICE-ITS UPGRADE
FOR LHC/PHASE-1