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L0 Project: Monitoring H1 Triggers with SpaCal

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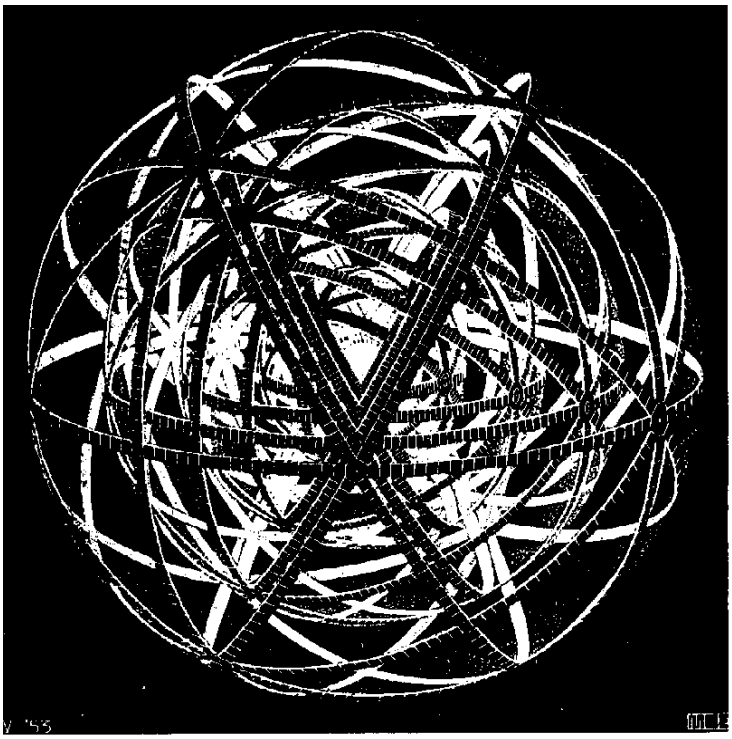

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Abstract[1]:
We have built a VME module using H1's ADC and BaBar TDC interfaced to H1's 29K processor. It is used to monitor SpaCal trigger, energy sums and trigger elements, by reading up to 130Kevents/s. The timing resolution is found to be surprisingly good (1ns) for energy sum signals. The performances under various beam conditions are shown, including a first study of the "hotspot" counters designed as a veto against e-beam background.

1 Introduction

The basic principle of our trigger monitoring system, called **"L0"** is:

- to set up a L0 channel for each L1 trigger element to be monitored,
- to define L0 thresholds below those of the corresponding L1 channels,
- to trigger on any channel above its L0 threshold,
- to read L0 channels (energy and time) and L1 trigger elements,
- to classify the L0 event and perform the relevant statistical analysis.

This system requires a high data acquisition rate and a private access to the main analog signals used and produced by the L1 trigger.

We use a proton-downstream detector (cf. "hotspot" in figure 1), in addition to the 3 SpaCal

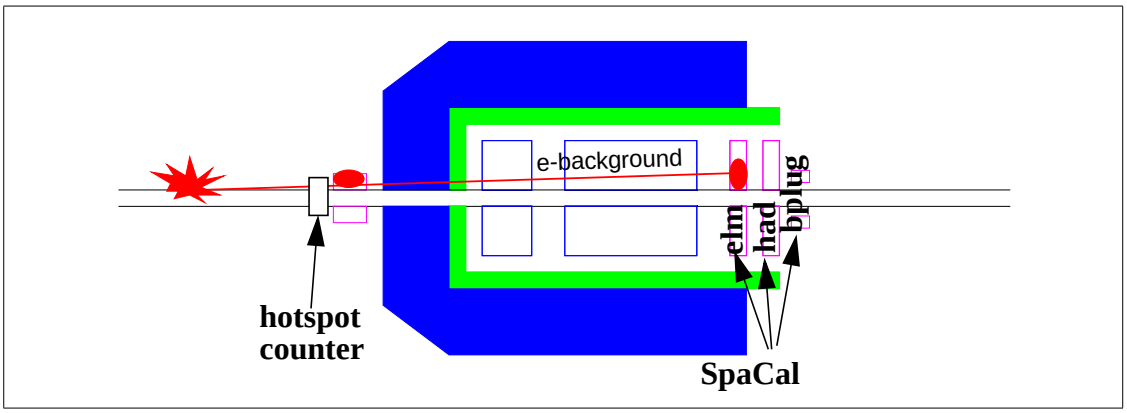

Figure 1: Position inside H1 of the detectors used by L0

calorimeters (electromagnetic, hadronic and backward plug) which are positron-downstream. This will permit to sort the 3 main classes of events: p-background, e-background and e-p collision.

[1] This note was written in 1997 as an H1 report. The L0 system was dismantled in 1998 in order to serve as a prototype for the upgraded HERA-TPol data acquisition which was setup by S.Schmitt. This DAQ is itself a prototype for the H1-luminometer/HERA-Polarimeters upgrades

2 Overview of the “L0” setup

The setup of our L0 monitoring system is described on figure2 . It is founded for one part

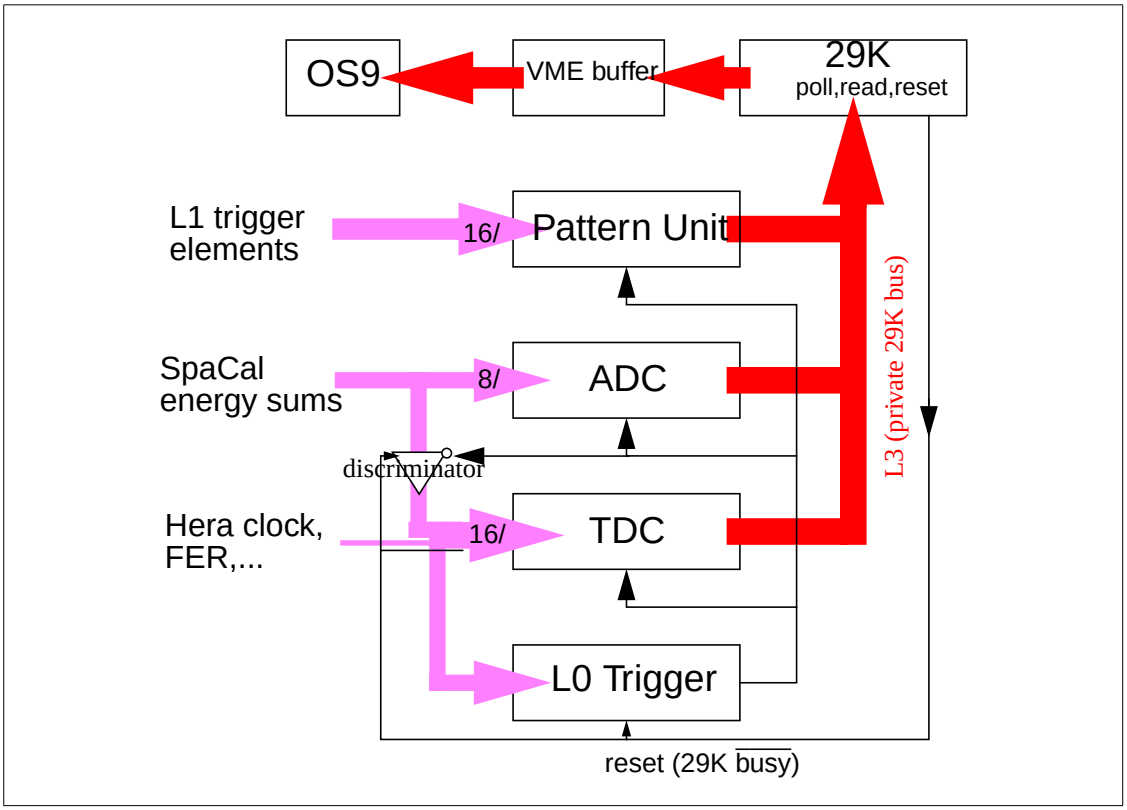

Figure 2: Overview of the “L0” SpaCal trigger monitoring system

on the real time 29K processor developped for H1, and for the other in the use of SpaCal energy sum signals, which yield SpaCal L1 trigger elements.
Its main elements are:

1. The OS9 VME card, which downloads the 29K processor and reads the VME buffer filled with data (events or histograms) by the 29K processor.
2. The 29K VME processor, which loops on a critical cycle: wait for event, read, fill histograms and reset-trigger.
3. The VME buffer. It is a CES 8232 module, just used as a memory.
4. The pattern unit, situated in the L0 VME card. It stores the 16 SpaCal trigger elements as 16 bits in a 32 bit word. The upper bit is set to 1 by a trigger signal, when the input lines are latched. This word is continuously polled during the wait-for-event phase of each 29K cycleThe ADC card, made by Saclay, which is the standard H1 calorimetry ADC. It has a VME format but needs an additional power supply which is connected through the L0 card. The 8 analog inputs are fed by 4 front panel connectors. The ADC readout is done by the L0 VME board through the J2 auxiliary bus of the VME crate.

The L0 card asks only one ADC conversion per event (8μs), as compared with the 128 conversions per event for a standard H1 DSP cycle (1ms).

5. The TDC which is a prototype chip made by LPNHE-Paris for the BaBar experiment. It is situated on the L0 card. It encodes 16 channels with a 0.5 ns step and an 8 consecutive hits per channel memory. Eight channels are corresponding to the 8 ADC inputs, 3 others to Hera clock / L1keep / 29K-reset, 5 are free. Inputs are gated by $\overline{29K\ busy}$. More about TDC will be found in [8.2].
6. The discrimators (CFD). They are ORTEC's NIM modules. Their NIM outputs are converted to ECL as well as other signals to be fed into TDC inputs.
7. The L0 trigger, on the L0 card. It is set by the OR of a subset of the TDC inputs and reset by the 29K reset. This trigger is sent, through different delays, to latch the pattern unit or to hold ADC signals, or to gate some TDC inputs.

3 Analog Signal Processing

We are using 7 analog signals:

- **6 SpaCal energy sums**: 3 "**ToF**" and 3 "**AToF**" (respectively 1 for the electromagnetic **elm** SpaCal wheel, 1 for the hadronic **had** wheel and 1 for the backward plug **bplug**),
- **1 hot-spot sum.**

3.1 Timing of analog signals.

They all have been cable-timed within a few nanosecond precision, using beam generated signals and / or electronic calibration signals. The 3 AToF signals and the 4 hot-spot counters have been timed with a proton beam, as shown on figure 3. Bplug was 60 ns early because

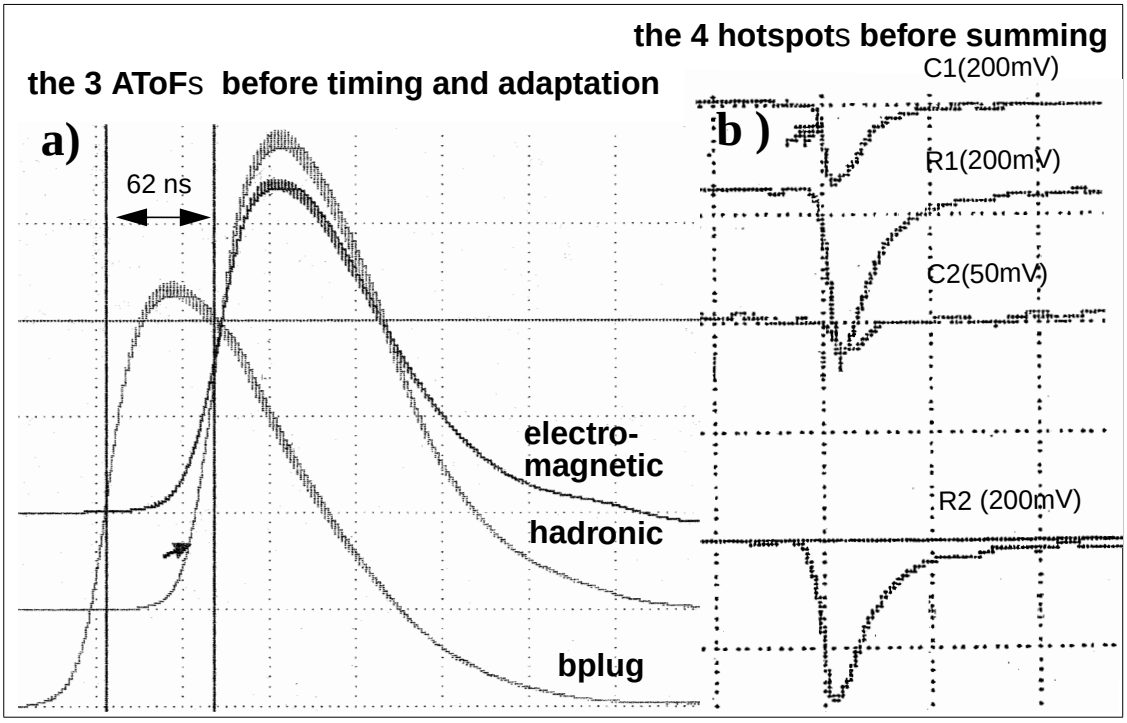

Figure 3: Averaged signals before timing and adaptation

of a cabling different from both SpaCal wheels. The 4 hot-spot counters were in time and showed no interesting correlation[2]. They were added, yielding the “hot-spot sum”.

3.2 Splitting and adapting the signals.

We used a passive method, which cost a factor four in ADC range (800 instead of 3600), because the active fanout did not perform up to the specifications:

- First the negative half of each bipolar 100Ω energy sum signal is used as the 50Ω input of the Ortec constant fraction discriminator (CFD).
- Second its positive half is used as the positive half of a bipolar input of the ADC card. It is adapted by a 50Ω resistor, because of the length of the cable joining the trigger rack and the L0 card (contrary to the standard H1 practice between ANRU and ADC). The result is seen by comparing the figure 3a, which has an unwanted reflexion of AToF signal, and figure 4a.

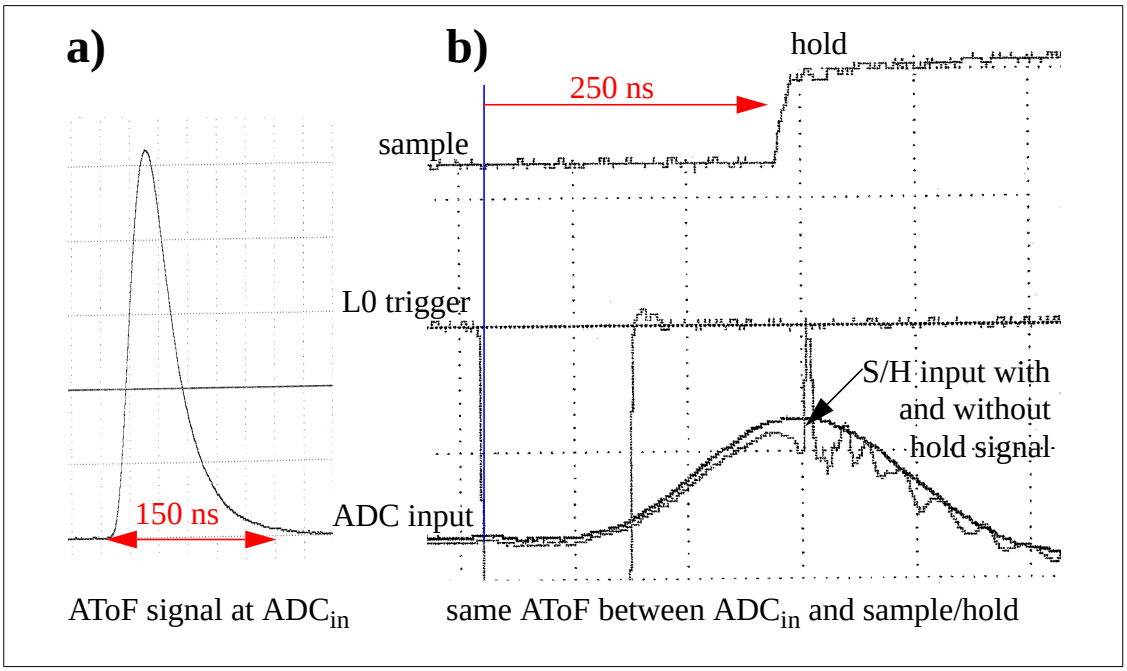

Figure 4: Energy sum signal before and after the input amplifier of the ADC board

3.3 ADC conversion.

The input receiver of the ADC card is not fast enough. It widens and delays the AToF signals. This feature turned out to be useful in order to adjust the timing of the hold signal produced by the L0 trigger as seen on 4b).

[2] There was no way to study the correlation between e-beam hotspot signals

4 The L0 card and the L0 crate

There are 2 versions of the L0 card:

1. a prototype used for this analysis.
2. a new version including features such as programmable delays δt_1 and δt_2 downloaded by VME.

The schematics can be found in figure 5. The readout characteristics, defined as register

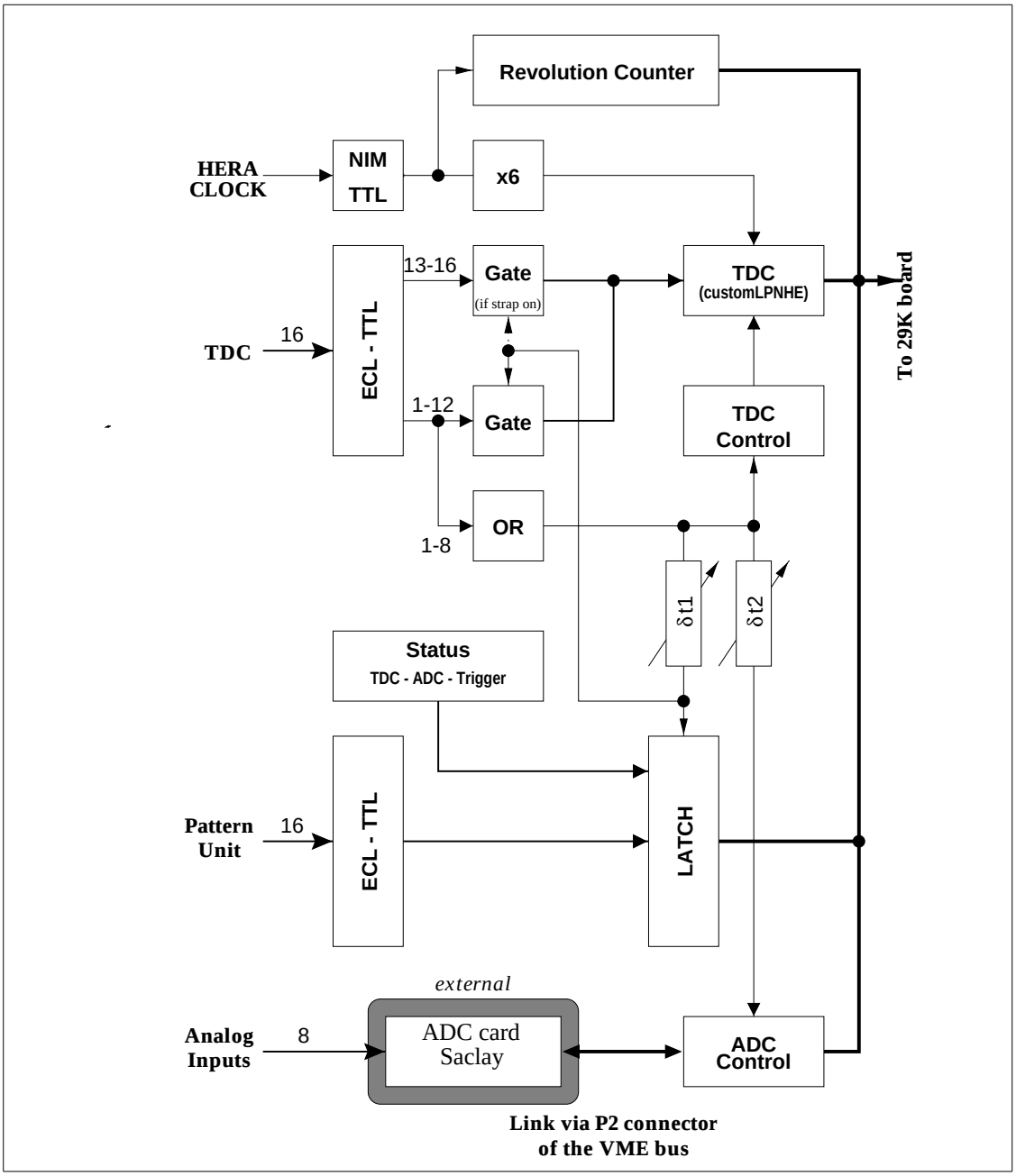

Figure 5: The L0 VME card

adresses on the private 29K bus (called “L3 bus”) are found in appendix[8.1].

Figure 6 shows the position of the L0 card in the L0 crate.

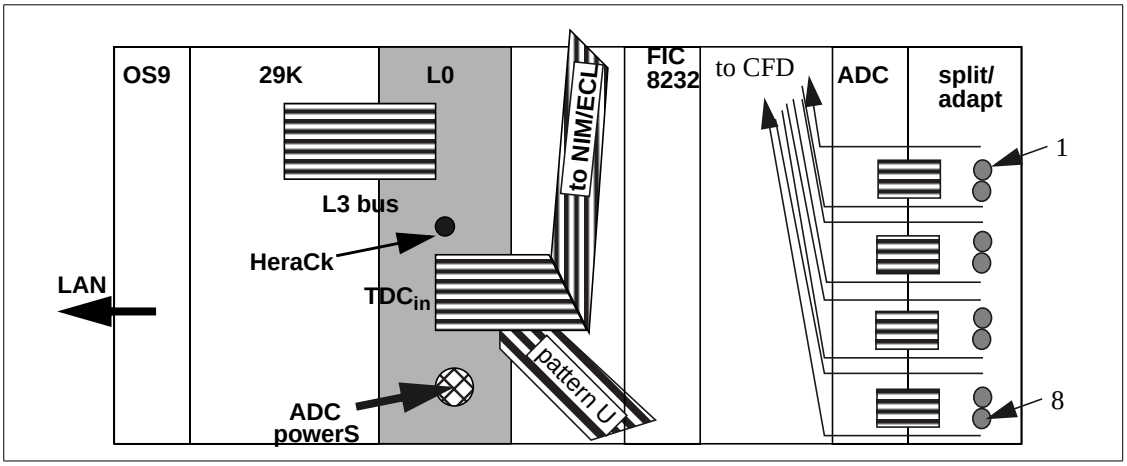

Figure 6: Setup of the L0 VME crate

5 Analysis of 1997 Runs

The L0 system was installed in May and June 1997. It was completed in July. Standalone runs were taken in July, September and October; during the latter runs genuine e-p events were collected. It allowed us to compare data taken with various beam and luminosity conditions and, for electronic tests, without beam.
Our analysis will proceed in three steps:

- first the study of the behaviour of the various encoders,
- second the classification of event types,
- third the information gained about HERA and H1.

5.1 The Clocks

The revolution counter (RC) counts Hera clock ticking, every 96 ns. Its value rc(i) is stored in a register when the trigger of event$_i$ arrives.
Two faster clocks are obtained:

1. by subdividing the Hera cycle into 6 “BaBar” cycles (with a PLL chip),
2. by subdividing the “BaBar” 16 ns cycle into 32 TDC steps (inside TDC chip).

Consequently the TDC clock has a period of 96ns / 6 / 32 = 0.5 nanosecond. It is counted by one counter inside the TDC chip, which is stored in the TDC memory whenever a leading edge is detected on any of the 16 TDC input pins. The TDC memory is organized in a 16x8 array, according to channel# & hit#.
The channel with a minimum TDC count [tdc$_{min}$(i)] is the one which is responsible for the trigger of the event$_i$. The maximum TDC count is bounded by the closing of the TDC gate , which happens a fixed delay after the trigger.

The TDC counter, being 16 bits wide, completes a revolution every 32.7 μs. This is enough to cover the spread of times measured for a given event, but not the time between consecutive events. By comparing rc(i) and tdc$_{min}$(i), one obtains one time stamp for each

event. We shall check that it stays synchronized with the Hera machine for the duration of a whole run.

5.1.1 the revolution counter.

1. event rates: By histogramming the difference of **RC**s between 2 consecutive events, we see in figure 7a) the Poisson distribution of the arrival time and we read on the

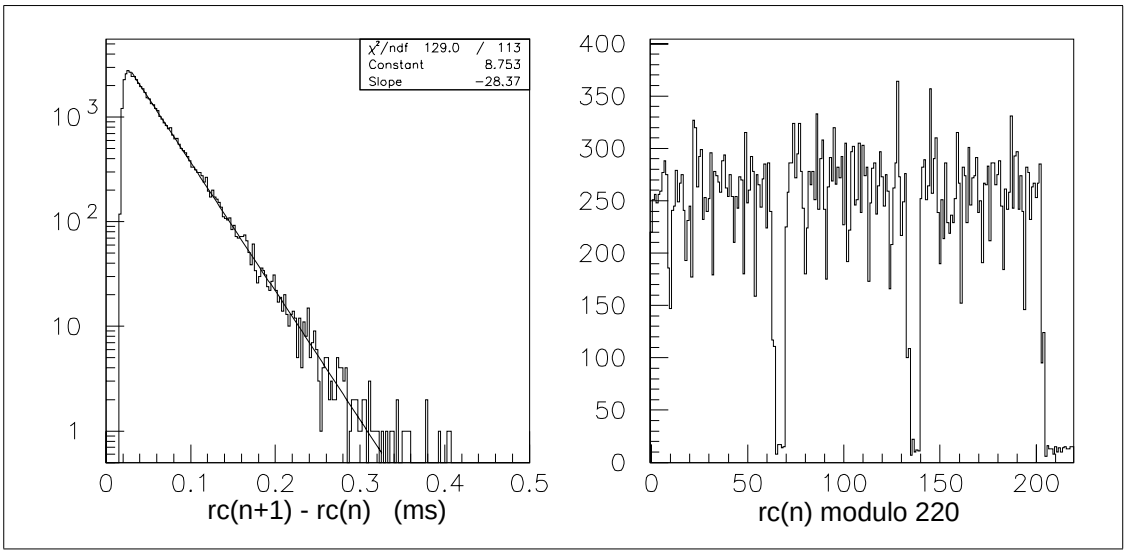

Figure 7: a) Time between events ; b)Number of events per bunch crossing

exponential fit the rate of events, which is 28.4 KHz. The hole of 20µs after t=0 gives the dead time, with a 96 ns resolution.

2. bunch ID: If the revolution counter stays in phase with the HERA machine which contains 220 bunches, the bunch number is equal to RC modulo 220.
The histogram of figure 7b) displays clearly the empty bunch structure of a HERA fill. This feature is useful in order to study the individual bunch properties.
3. RC counting bug: when adjusting the RC and TDC clocks, one finds that the RC counter is affected by some jumps, followed by a reverse jump. The value of the jump is 2^n and it happens only when the trigger occurs at a specific time within a Hera cycle [$tdc_{min}(i) = k$ ns *modulo*{96 ns}]. This is due to storing the RC counter at the exact moment when it is incremented by a Hera clock edge. The knowledge of the constant k is useful when comparing rc(i) with $tdc_{min}(i)$.
4. synthesis of a **big clock:** The RC is passing through 0 every 2^{32} Hera cycle, i.e. every 412.3 seconds. Assuming that this duration exceeds the possible gap between 2 events, we can detect each gap during which RC passes through 0. We create a "big clock" counter in a 64 bit word, by adding 2^{32} to the RC when RC=0 and rescaling it in such a way that less significant bits coming from the TDC clock can by added to it. This is the most convenient time stamp.

5.1.2 the hera clock

Due to the multihit capability of our TDC, each positive edge of the Hera clock is timed and stored in the TDC chip until the TDC gate is closed (i.e. $\delta_1 \cong$ 300 ns after the trigger, cf. fig.5).

1. hera period: We digitize up to 8 consecutive edges of Hera clock and check if the time differences stay in one 0.5 ns bin. This constitute a good test of the system.
2. check of the revolution counter: The last Hera clock edge to be digitized (read first) tags the Hera cycle during which the TDC gate was closed. We can conveniently take it as a Hera synchronous t_0 + 3x96 ns. However we have first to determine precisely the position of the TDC gate relative to the Hera clock if we want to know how many clock edges -2 or 3- have been digitized during the δt_1 delay.

5.1.3 the 29K reset

A TDC channel has been attributed to the 29K reset which is digitized at the exact time where, at the end of the processing of an event the 29K busy is reset. This gives the duration of the $\overline{busy}$ state $tdc_{min}(i) - tdc_{29Kreset}(i)$. The processing time of the previous event is $tdc_{29Kreset}(i) - tdc_{min}(i-1)$.

5.1.4 the L1keep

There are 3 possibilities:

- An event seen by H1 central trigger has deposited energy in SpaCal when the L0 system is waiting for an event. Then we have both a L0 and a L1 trigger, coming 2.2 μs after L0. The difference between the L1 and the L0 latency times is seen in fig.8 a). This detects occasionally some L1 triggers coming one bunch crossing too late[3].
- An event during L0 dead time.
- An event not seen by L0 trigger (usually generated by other subdetectors, since L0 thresholds are below L1's).

In all cases L1keeps are recorded in the TDC, because of its multihit capability. It is verified that L1keep comes at a unique position within the Hera cycle (fig.8 a). The analysis of L1keep gives the probability of firing L1 trigger after a given SpaCal trigger element.

5.2 The TDCs

The functions of our "BaBar" TDC are described in the appendix [8.2]. The resolution and the stability of this TDC are known from electronic test bench results to be respectively 1 and 0.2 LSB (1 LSB= .5 ns). Our experimental results in H1 are compatible with this resolution, as seen on figure 8 and 9

Practically we create an origin of time for each event, which is the beginning of the HERA cycle containing the first TDC hit of this event.

Then we correct each TDC hit corresponding to an ADC channel by the slew time computed as a function of the ADC value. The slew-corrected time takes a 0 value for a "standard" event (e.g. 0 ns for a proton remnant hitting the hotspot counter and 40 ns for an electron background). Figure9 shows the TDC response on SpaCal e-p or beam-gas events.

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[3] This fact is confirmed by offline analysis. These late triggers are not those due to SpaCal calibration by light pulses (the only ones which should come late).

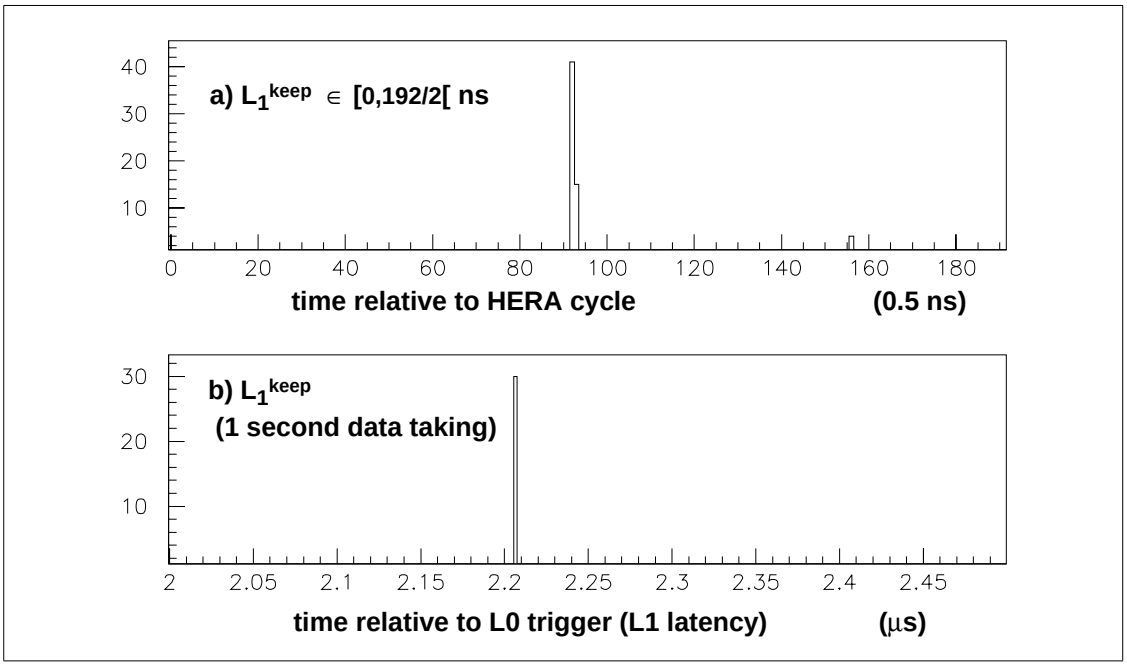

Figure 8: Time of L_1^{keep} signal a) within a 96 ns Hera cycle; b) after the L_0 trigger

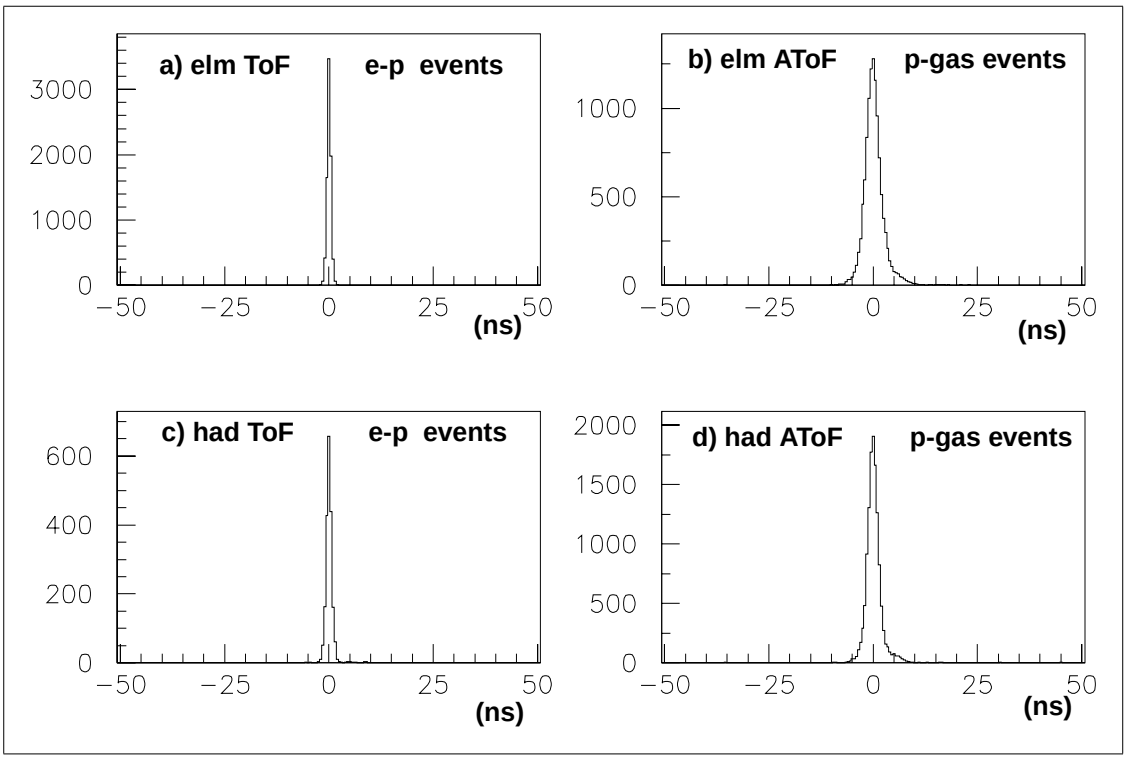

Figure 9: TDC distribution for the energy sums signals of **elm** and **had** SpaCal wheels, after **ToF/ AToF** time of flight filtering done by the frontend electronics

5.3 The ADCs

The encoding time of the ADCs is around 8 μs. Most of this time is lost for the L0 data acquisition. However it could be used for TDC readout.

The dynamical range of analog pulses has been divided by 4 as said earlier. We see in figure 10 adc counts limited to 550 instead of 4095. This should be cured by a correct analog

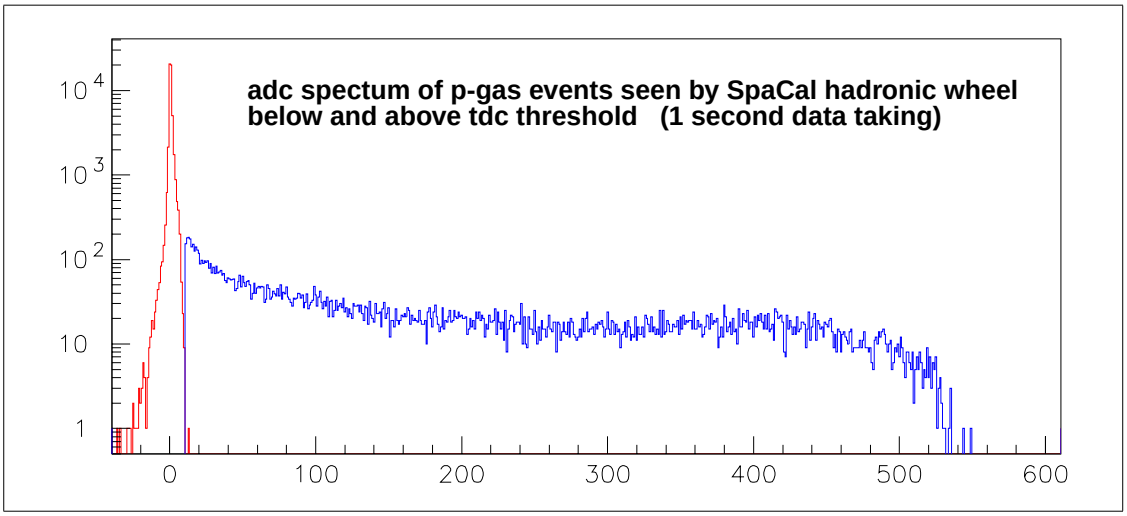

Figure 10: Exemple of ADC Spectrum. Pedestal events (red) are due to hotspot L0 triggers

receiving electronics.

5.4 The Pattern Unit

not processed yet

5.5 Event Types

The analysis of L0 events leads to an almost non ambiguous classification of all H1 events. These few classes should be useful for the monitoring of the H1 environment and its trigger response. They are constituted by all combinations of “in-time” (ToF) and “out-of-time” (AToF) response of 4 detectors: the electromagnetic, hadronic, backward plug SpaCal wheels and the hotspot counters.

At first we see an abundant contribution of nonsensical ToF ∩ AToF hits in the same detector, due to our low threshold discriminators firing on weak cross-talk signals. We shall solve this ambiguity by comparing the ToF and AToF energy sums as shown in the next paragraph.

5.5.1 ToF/AtoF separation by energy difference

The comparison of ToF and AToF total energy sums is done by an algebraic formula. For instance we can mimic the comparison done in hardware by the L1 trigger element logic and define:

- a ToF flag $\leftrightarrow$ $E_{tot}^{ToF} - E_{tot}^{AToF} > 600$ MeV
- an AToF flag $\leftrightarrow$ $E_{tot}^{AToF} - E_{tot}^{ToF} > 600$ MeV

This flag is meaningful, as seen in figure 11 when we compare the timing of the AToF energy sum of the electromagnetic wheel for the 2 classes of event. For real p-gas events which are well flagged “AToF”, the pulses are coming 10 ns earlier than for ToF flagged events. This is

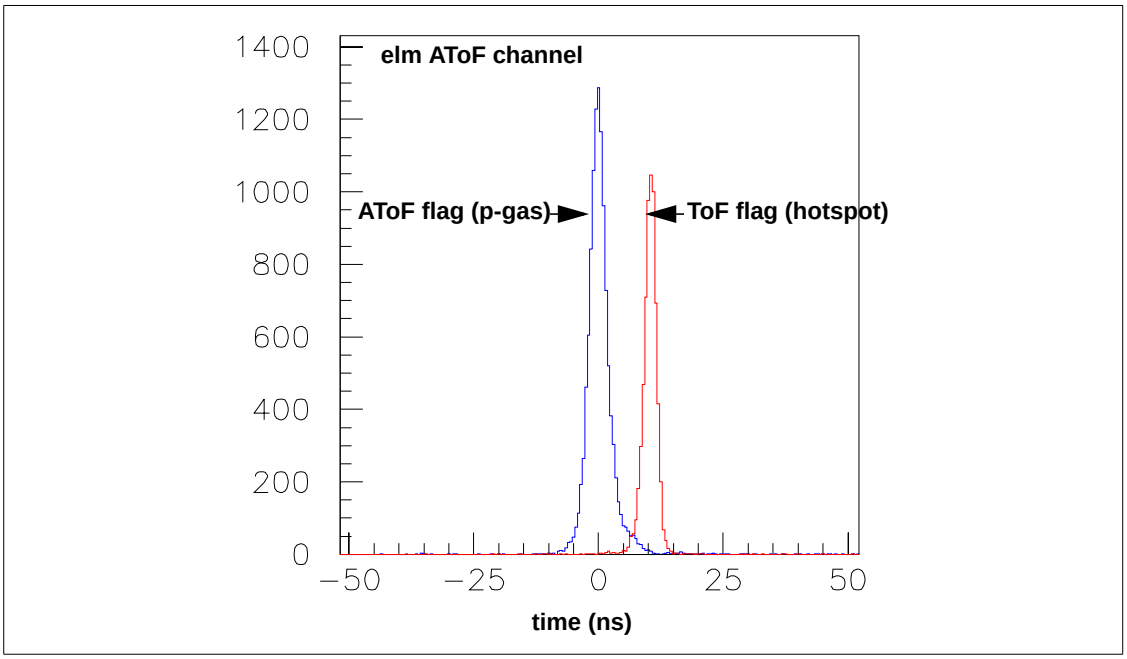

Figure 11: Time of flight distribution for elm AToF signals. AToF events (blue at t=0) and ToF events (red at t=+10 ns) are separated by energy difference criterion.

consistent with the fact that some of the energy of e-background (hotspot) or real e-p events is leaking in the AToF channel, but with the timing of ToF events.

5.5.2 Event classification

We have counted for each event in a typical lumi run the main combinations of the 5 SpaCal flags:

Rates(lumi run)	electromagnetic	hadronic	backward plug
ToF single hit	7486	1339	
ToF double hit	737		
AToF single hit	1367	1283	439
AToF double hit	2414	1512	
AToF triple hit	7607		

The ToF∩AToF coincidences have been neglected because they represent only 0.1%. (This is another justification of the ToF / AToF separation criteria introduced in the previous paragraph).

Now, if we look at hotspot counter, it is associated with spacal in 50% of the cases with rates as shown in the next table.

Rates(lumi run)	ToF	AToF
no hotspot	9171	10777
hotspot	391	3871

5.5.3 Coincidences ToF/hotspot and AToF/hotspot

For the 2 well defined classes of SpaCal events (ToF and AToF), we can look at the time distribution of hotspot hits (cf. figure 12):

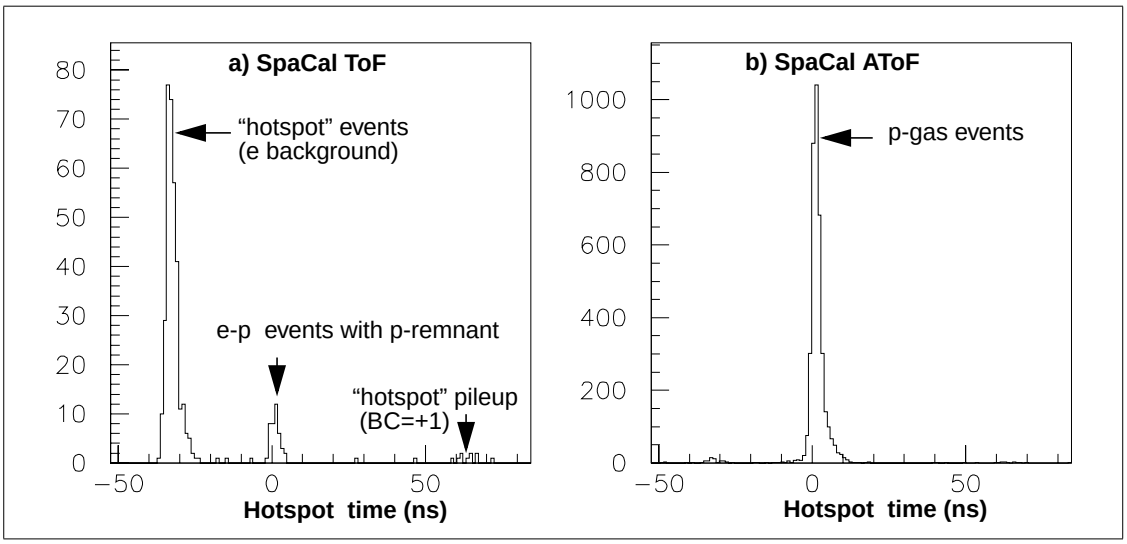

Figure 12: Hotspot TDC time for events in coincidence with SpaCal a) flagged ToF; b) AToF

- SpaCal ToF and early (-40 ns) hotspot hits. This is the real signature of e-beam background known as hotspot
- SpaCal ToF and on time (0 ns) hotspot hits. This is an e-p collision with a remnant hitting the hotspot counter.
- SpaCal AToF and on time (0 ns) hotspot hits. This is a p-gas collision upstream of SpaCal seen by one or more SpaCal wheel, with very forward proton fragments hitting the hotspot counter.

Besides these 3 classes, there is very little background, most of it looking like random pileup events.

6 Conclusion

6.1 Hardware

The hardware of our L0 system fulfills its 2 main purposes:

- a good time and energy resolution on the SpaCal energy sums. The time resolution of around 1 ns is surprisingly good considering the great number of channels contributing to this sum.
- a fast readout using a bloc transfer of data on the 29K system bus. To make a good use of this intrinsic speed, one should optimize the software.

It presents an important drawback:

- an ADC with a long (8 μs) conversion time.

Without this long conversion, our DAQ would work at rates >100Khz.
The BaBar TDC chip that we have been the first to use, is more practical that the TMC used in H1, because it has no dead time and a resolution better by a factor 2.

6.2 Analysis of H1 trigger environment

Due to the capability of L0 to read 1000 times more events per second than H1 central DAQ and the fact that a majority of background and physics events are seen by our SpaCal L0 trigger, we have an unbiased and almost complete sample of all what goes through the H1 detector.
We have found essential to read a forward timing detector, the “hotspot” array of scintillator placed near to the forward “plug” calorimeter. In coincidence with SpaCal, it subdivides the HERA background into an e-induced sample and p-induced one. These type of counting rates are already available in the counting room from other sources. The advantage of the L0 rates is that they are directly related to the main H1 trigger elements and that they monitor trigger efficiencies.
Unexpectedly the hotspot-SpaCal coincidence yields a very clean e-p signal due to the proton remnant. With our good timing efficiency it is clearly separated. Here again it has the advantage of being directly related to H1 trigger.
L0’s very good timing accuracy could also be used for locking the phase of the HERA machine relative to the phase of the SpaCal ToF windows which are a critical ingredient of H1 trigger (or also lumi in conjunction with satellite structure of p-bunches).

7 Acknowledgements

The authors thank the Paris BaBar group, in particular P.Bailly, J.F.Genat and H.Lebbolo for their invaluable help in the best use of their TDC chip.

8 Appendices

8.1 L0 card readout

Registers accessible through L3 bus (read only):

- **RESET**0x400010reset TDC, revolution counter.
- **READ_PU**0x400000read status word and Pattern Unit.

pattern unit data format:

TRIG		ADC	CALOK	PATTERN UNIT
D31		D17	D16	D15 D0

TRIG	1	trigger arrived (logical OR of TDC 0...7).
	0	waiting for trigger
ADC	1	ADC conversion active
	0	ADC conversion over
CALOK	1	TDC calibration over
	0	TDC uncalibrated, dont use it

- **READ_RC**0x400014reads HeraClock Revolution Counter
- **RESET_INPUT**0x40000Cunlocks TDC, PU and ADC inputs.
- **READ_ADC**0x400004reads Saclay ADC data, then points to next channel

ADC data format:

channel number	ADC data
D15 D12	D11 D0

- **READ_TDC**0x400008reads TDC data, then points to next hit or 1st hit of next channel

TDC data format

END	VALID		Channel #	OVER	UNDER	COARSE	VERNIER
D31	D25		D21 D18	D17	D16	D15 D5	D4 D0

FIN	0	more data to read
	1	last data
VALID	0	data valid
	1	data not valid
Channel#	0...F	channel number
OVER	1	Vernier Overflow
UNDER	1	Vernier Underflow
COARSE		16 ns steps counter
VERNIER		500 ps steps counter

8.2 TDC chip

The TDC chip contains 16 channels, 8 hits per channel. TDC data are made by counting a “BaBar clock”, which is obtained by dividing each Hera cycle in 6 BaBar cycles, using a commercial PLL chip. The TDC chip interpolates the BaBar clock, subdividing a BaBar cycle into 32 steps of 0.5ns. For pulses arriving at the critical time when the TDC receives a BaBar clock edge, we have to take into account the “underflow” and “overflow” bits in order to correct the TDC data.

BaBar TDC chip. Package: PGA 120. (Authors: P. Bailly, J.F.Genat, H.Lebbolo, Zhang Bo)			
Pin	IO	Name	Function
A1	I	S0	Time input. Positive edge sensitive. Minimum pulse length 3ns. Next positive edge occuring before 32ns is not measured.
B3	I	S1	
C4	I	S2	
A3	I	S3	
C5	I	S4	
A4	I	S5	
C6	I	S6	
A6	I	S7	
B7	I	S8	
B8	I	S9	
B9	I	S10	
C9	I	S11	
B11	I	S12	
C10	I	S13	
B12	I	S14	
C11	I	S15	
C7	I	Ck	59.5 MHz Clock.
C12	O	Calok	End of calibration process. Set to high when calibration successful.
D11	I	Calin	Calibration request. Negative edge sensitive. One clock period minimum width.
B13	I	Clear	Coarse counter clear. Active low. One clock period minimum width.
C13	I	Reset	Reset. Clears verniers, coarse counter, FIFO’s, calibration values, and control. Active low. One clock period minimum width.
D12	I	Cs	Chip Select. Enables data onto the data bus. Active low.
D13	O	Pwre-set	Power on Reset. Resets at power on. 164 ns duration for 0.5 ms power risetime.Should not be used as input.
E13	I	Sd0	Select Data -> 00 Time data; 01, 10, 11 Tests
E12	I	Sd1	

E3	O	FE0	FIFO empty flags. Active true. Active after Reset. Positive edge synchronized on Read. Negative edge on Write FIFO (P0-P15<>0). FIFO depth: 8 words
E2	O	FE1	
E1	O	FE2	
F3	O	FE3	
F1	O	FE4	
G2	O	FE5	
G3	O	FE6	
H1	O	FE7	
J13	O	FE8	
H11	O	FE9	
H13	O	FE10	
G12	O	FE11	
G11	O	FE12	
G13	O	FE13	
F12	O	FE14	
F11	O	FE15	
N6	O	D0	Data output. D0-D17 (D0 LSB=500ps). Tri-state outputs controlled through Cs.
M7	O	D1	
N7	O	D2	
N8	O	D3	
M8	O	D4	most significant bit of TDC vernier
L8	O	D5	less significant bit of TDC’s BaBar clock counter
N9	O	D6	
M9	O	D7	
N10	O	D8	
L9	O	D9	
M10	O	D10	
N11	O	D11	
N12	O	D12	
L11	O	D13	
M11	O	D14	
N13	O	D15	most significant bit of TDC’s BaBar clock counter
K11	O	D16	vernier underflow. On vernier underflow, subtract 1 to coarse value and set vernier values to 31.
L12	O	D17	vernier overflow. On vernier overflow true, add 1 to coarse value and clear vernier values. Actual range is so 16 bits.
L13	O	D18	D18-D21 channel address 0 to 15. True logic.
J11	O	D19	
K13	O	D20	
J12	O	D21	

BaBar TDC chip. Package: PGA 120. (Authors: P. Bailly, J.F.Genat, H.Lebbolo, Zhang Bo)			
M5	I	Rad0	Read address input. Should be stable 5 ns before and after Read for data output. True logic (Rad0 = LSB).
N5	I	Rad1	
L6	I	Rad2	
M6	I	Rad3	
N4	I	Read	Enable data onto the data bus. Data appear 10ns after negative edge.
H2	O	P0	Write FIFO output pattern. Synchronized on 59.5 MHz clock. Pulse width: one clock period. Activated on the next clock period following a time input. Active high.
H3	O	P1	
J1	O	P2	
J2	O	P3	
J3	O	P4	
K2	O	P5	
L1	O	P6	
M1	O	P7	
L3	O	P8	
M2	O	P9	
N2	O	P10	
L4	O	P11	
M3	O	P12	
N3	O	P13	
M4	O	P14	
L5	O	P15	
C1	I	Bist	BIST test input. Should be tied low in run mode. High level enables the BIST test.
C2	O	Orstart	Or function of the start inputs. Used for tests.
D3	O	Orstop	Or function of the stop inputs. Used for tests.
B2	I	G0	Weight for calibration steps. (G0 LSB). True logic. Should be set to 10 in run mode.
B1	I	G1	
A2		Gnd	
A5		Gnd	
A8		Gnd	
A11		Gnd	
A13		Gnd	
F13		Gnd	
K12		Gnd	
M12		Gnd	
N1		Gnd	
L2		Gnd	
G1		Gnd	
D2		Gnd	

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B4		Vdd	
A7		Vdd	
A9		Vdd	
A12		Vdd	
E11		Vdd	
H12		Vdd	
M13		Vdd	
L11		Vdd	
L7		Vdd	
K3		Vdd	
K1		Vdd	
F2		Vdd	
C3		Vdd	
D1		NC	
B5		NC	
B6		NC	
C8		NC	
A10		NC	
B10		NC	

The rule for computing time from TDC raw data is:

OVER = 0 and UNDER = 0	ΔT = 16ns x COARSE - VERNIER x 500ps
OVER = 1 and UNDER = 0	ΔT = 16ns x (COARSE-1)
OVER = 0 and UNDER = 1	ΔT = 16ns x (COARSE+1) - (31x500ps)