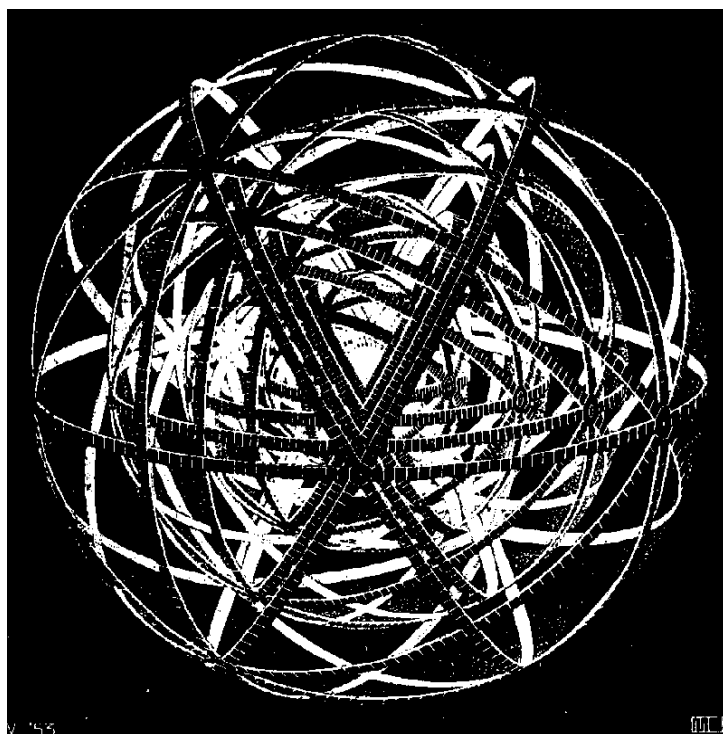Laboratoire de Physique Nucléaire et de Hautes Énergies
CNRS - IN2P3 - Universités Paris VI et VII

Test of Skydice CLAP electronics

E. Barrelet

4, Place Jussieu - Tour 33 - Rez-de-Chaussée
75252 Paris Cedex 05
Tél.: 33(1) 44 27 63 13 - FAX: 33(1) 44 27 46 38

1 Introduction

This report describes the test of the CLAP readout electronics done for the commisioning the Skydice instrument. The CLAP hardware consists of a) the **C**ooled **L**arge **A**rea **P**hotodiode (Hamamatsu S3477), b) a **FE_box** containing the frontend electronic board and the CLAP, c) a **BE-box** containing the backend electronic board, d) a PC readout of the BE-box through a USB interface. The tests reported here concern a prototype version of the CLAP electronics delivered in July 2011. A final version of both FE and BE boards are expected for end of october 2011.

The emphasis of this report is centered on the features of the BE electronics which were lacking in the previous SNDICE system: the waveform recording using a local digitization clock, the FIFO providing an 8 Megasample record length and the USB-2 link transfering data to the PC (the transfer rate is more than twice faster than the digitization rate).

We shall design some digital signal processing methods taylored for high-precision, large-range, long-duration and multiple signal sources.

For most of the study of FE electronics, we rely on the reference [1], a study of the SNDICE ASIC preamp using the Tektronix DSA digitizer and covering a very large frequency range from 1 GHz to a fraction of herz. The frequency range above 250 kHz was studied again using the DSA, but the lower frequency range was studied using the new CLAP digitizer itself.

Therefore logically our plan starts with a presentation of the whole system. Then we study the backend part and finally the frontend part. For each part we study firstly the noise which limits the precision of the instrument in view of its high sensitivity and secondly the calibration which limits the accuracy of the measurement.

2 Overview of CLAP electronic system

The design of the digitizer electronics in the Back-End box is shown in Figure 1.

It is fed by a single power supply from which all positive and negative voltages needed in this card and the frontend card are made. It contains three sections all controlled by a FPGA:
1) the USB interface developed by LAL,
2) the digitizer itself made of a multiplexer (8 out of 16 channels are used) and a 16 bit ADC,
3) the 16 Mbyte FIFO storing up to 2^{23}-2^{10} consecutive samples, i.e. more than sixteen seconds at maximum digitization rate.

The backend card is connected by a flat cable to the Frontend box which design is seen in Figure 2.

Inside the frontend box, the ultralow current amplifier has been studied independently with a fast low noise digitiser (Tektronix DSA).
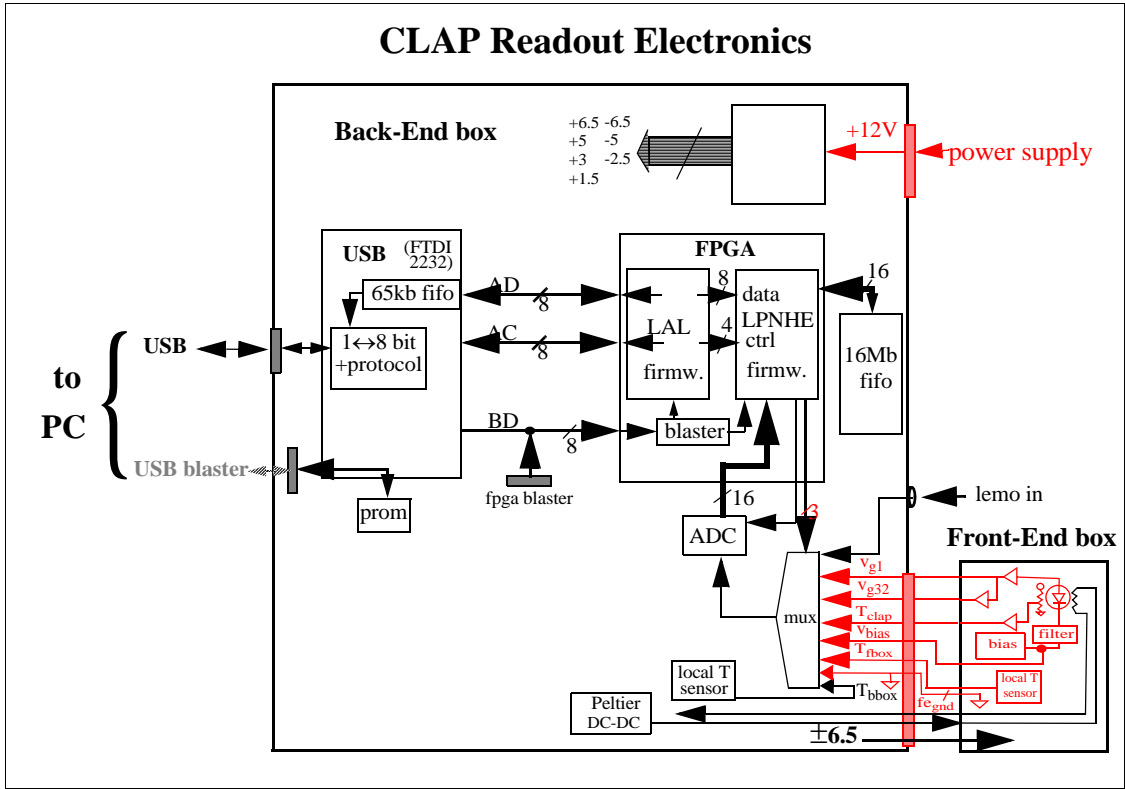
Figure 1: Overview of the CLAP electronic system

3 Test of BE-box

3.1 Tuning input impedance

The first test consists in checking the ADC using the lemo input which gives direct access to the digitizer through the multiplexer. Initially we have seen that the multiplexer was not really transparent. It could introduce large offset or non linearities when its inputs or its power supplies were outside specified values. The values of input impedance of each channel have repercussion on the size of cross-talk observed when switching from one channel to another. We started by sending a square wave generator signal in the lemo input. This yields a 50% x-talk in other channels when they are at high input impedance. When strapped to ground there is still a 9% x-talk at 250 kHz (125 kHz per channel) decreasing to 4% at 125 kHz and 2.5% at 64 kHz as seen in Figure 3. It is impossible of course to strap these inputs. We shall more likely will adjust input impedance in a range compatible with the signal source, say 1 kΩ. Then this cross-talk study will have to be redone, as well as the bandwidth of the channel will be adjusted. In the case of the lemo input the bandwidth is presently limited by the digitizer itself. Presently the risetime limit is a firmware one (4 µs). The true hardware limit due to the adc max rate is 2µs.
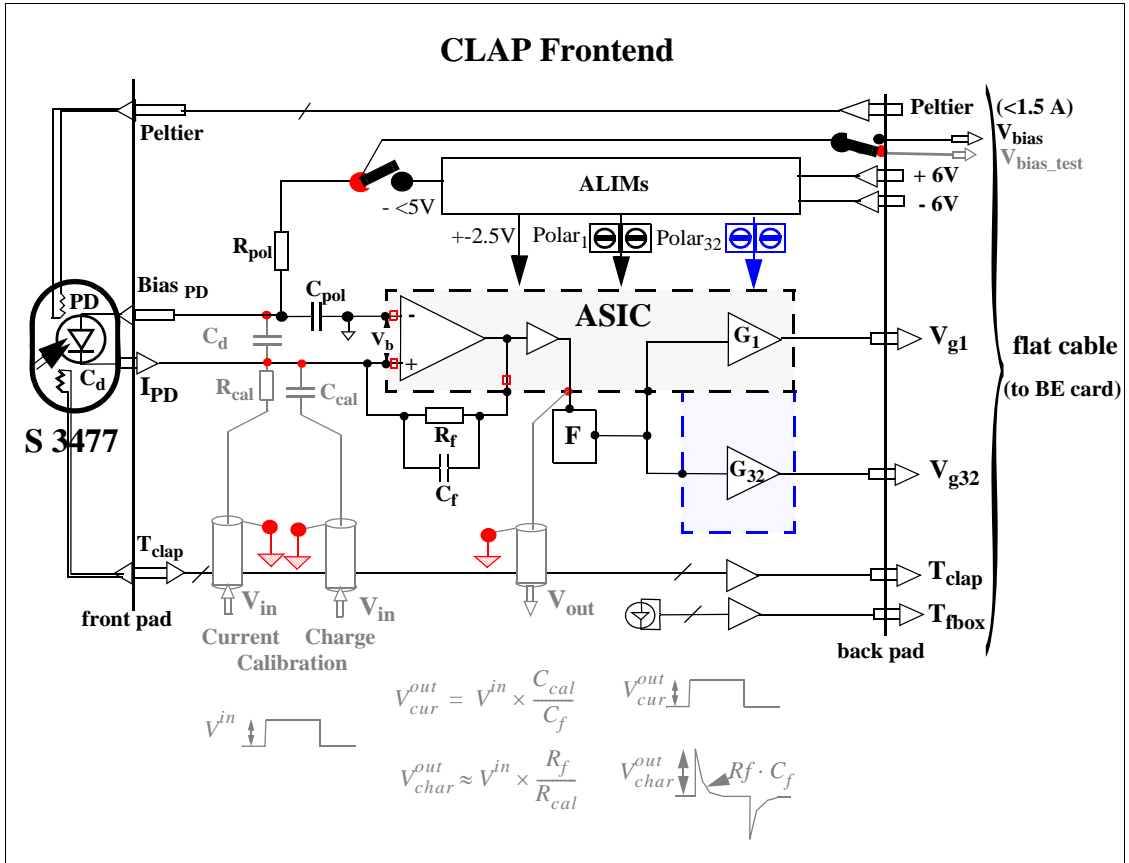
Figure 2: Detailed setup of CLAP Frontend electronics. In grey the specific calibration parts which are removed during normal operations.

3.2 Study of the lemo channel pedestal (0 Ω input)

When grounding the lemo input, one should measure only the internal noise of the adc and its input multiplexer. The average signal should be null. Figure 4 shows that the average pedestal is 3 adu (0.3 mV). The noise is gaussian, around 0.7 adu (RMS), which is typical of the digitization noise, plus a small contribution in non gaussian tails. The FFT spectrum shown in Figure 5 confirms this hypothesis -notably that the digization noise is white (flat spectrum)- and that an other contribution exist below 10 kHz.

By applying a 10 kHz digital filter to the waveform as shown in Figure 6 one discovers the nature of this extra noise. It is made of spikes occuring roughly every 0.1 second but not regularly. It could be due to the PC connected to the box through USB link.

### 3.3 Digitizer calibration (lemo constant level input)

Figure 7 shows the setup used for calibrating the digitizer section of the Back-End box. It is conceived for a low pickup noise operation and a good DC monitoring with a 4-5 digit voltmeter. The voltage drop in the BNC cable (=$R_{BNC}/50$) is 0.3%. The only «visible» noise (besides the ADC noise seen in 3.2) is a 0.15mV ripple at 100 hz most likely due to the voltage source. A technique was developed to deal with this ripple which merits more exposure, because it seems simple and better adapted for suppression
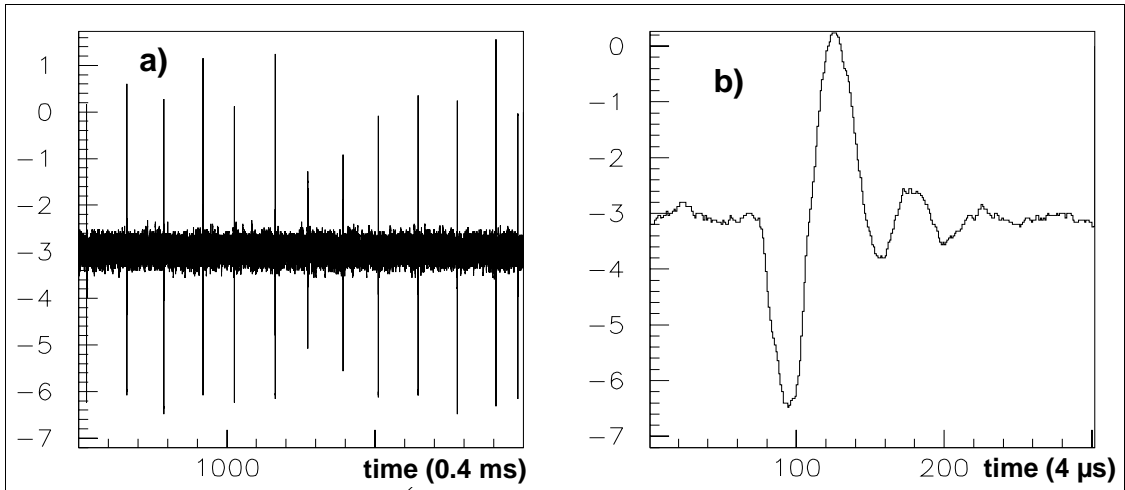
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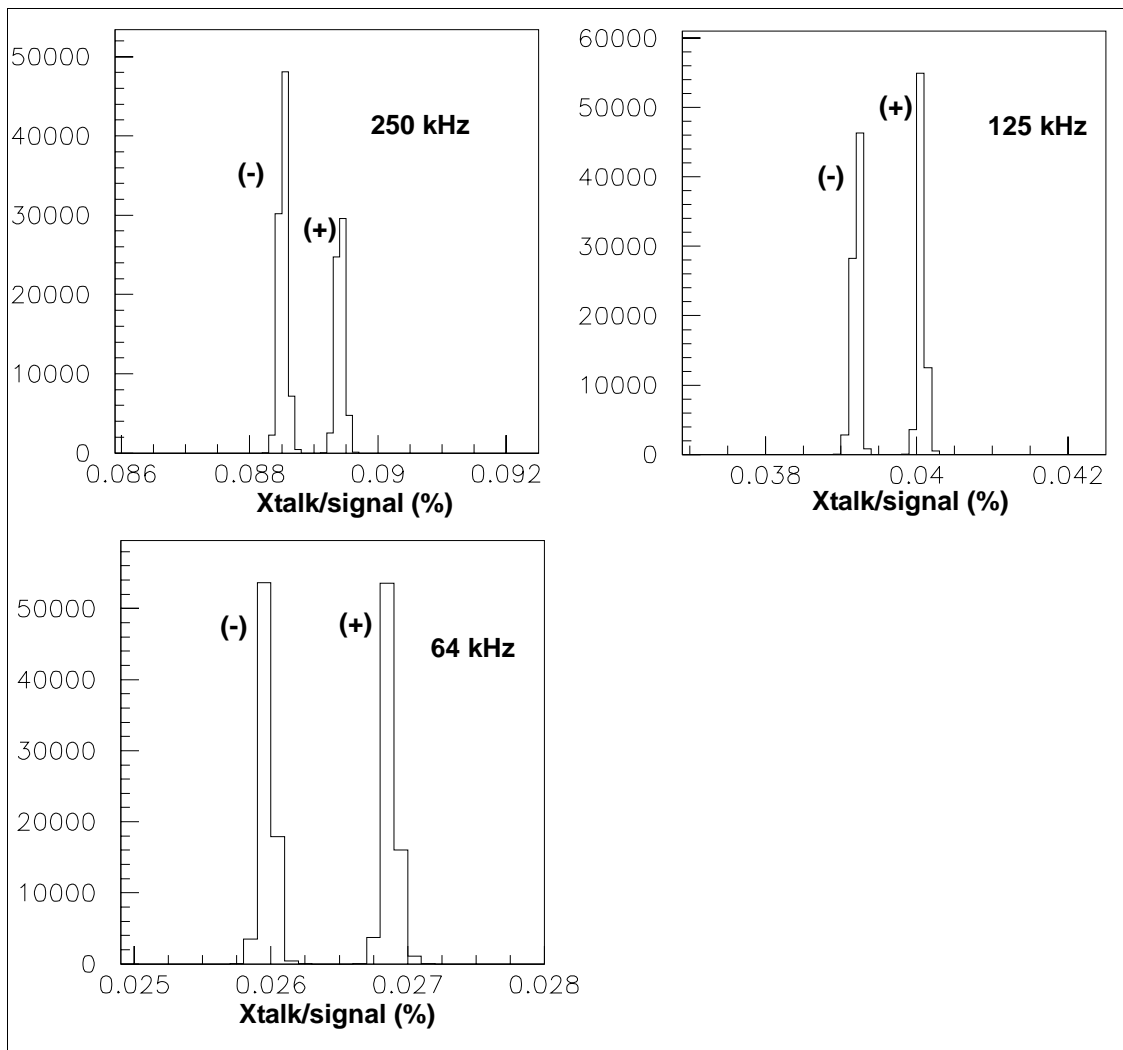
Figure 3: Ratio Xtalk/signal for 250 kHz, 125kHz and 64kHz sampling rate. one peak for each polarity at one volt amplitude.
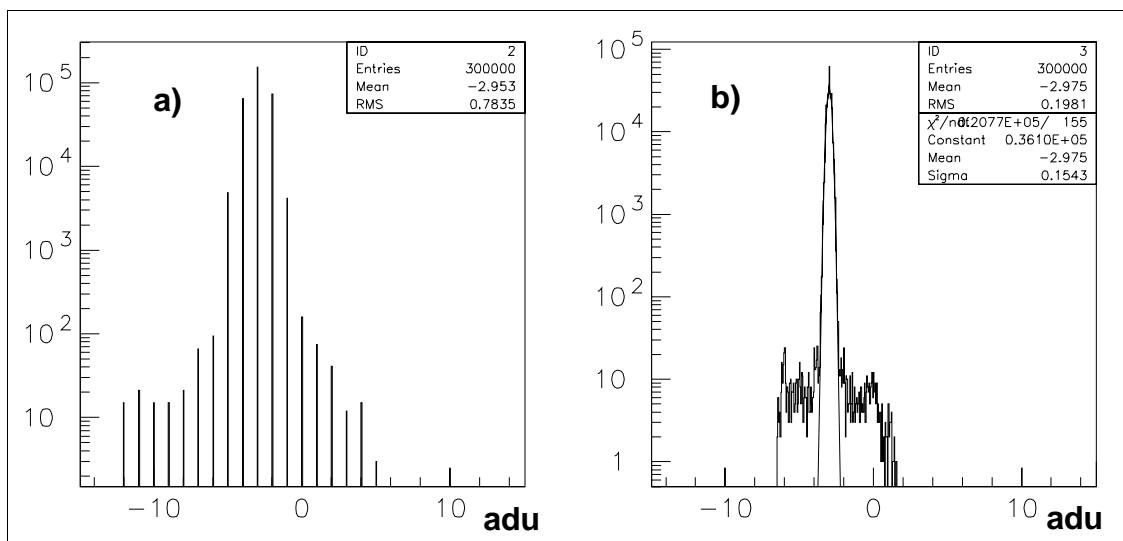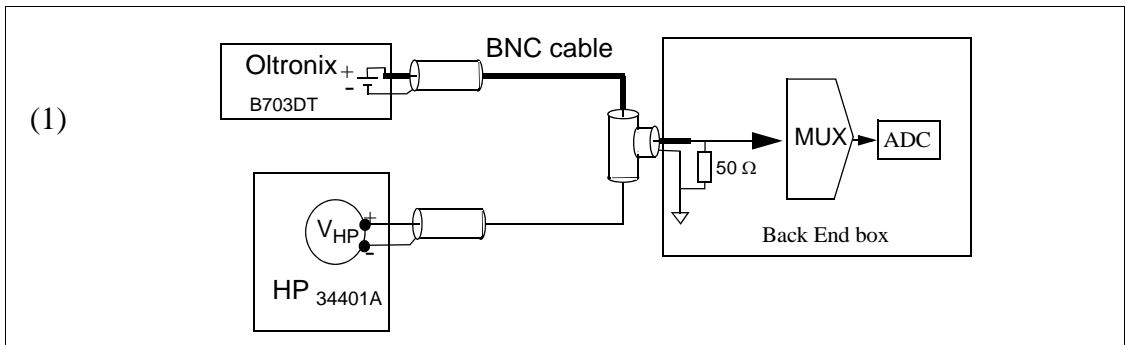

Figure 4: Lemo grounded input: Fluctuations of digital signal **a)** raw ADC; **b)** after filtering at 10 kHz
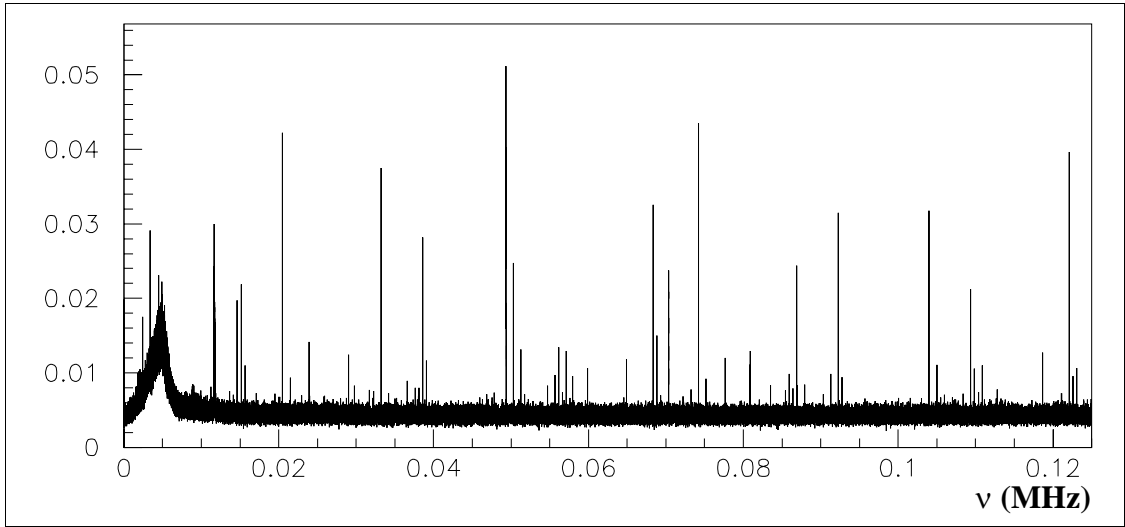
Figure 5: Frequency spectrum of lemo input grounded by a 0 Ohm resistor («pedestal»)

**Figure 6:** Lemo grounded input filtered signal: **a)** One second record; **b)** zoomed on one spike

Figure 7: The calibration setup of the CLAP backend Digitizer : a power supply, a multimeter connected by a low resistivity BNC cable to the lemo input of the Backend box .

of 50 Hz (or any stable synchronous noise) that the «power cycle» technique used by Keithley.

3.4 Cyclic noise auto filtering

The concept of the auto-filtering can be represented (in Figure 8) as a χ^2 fit comparing
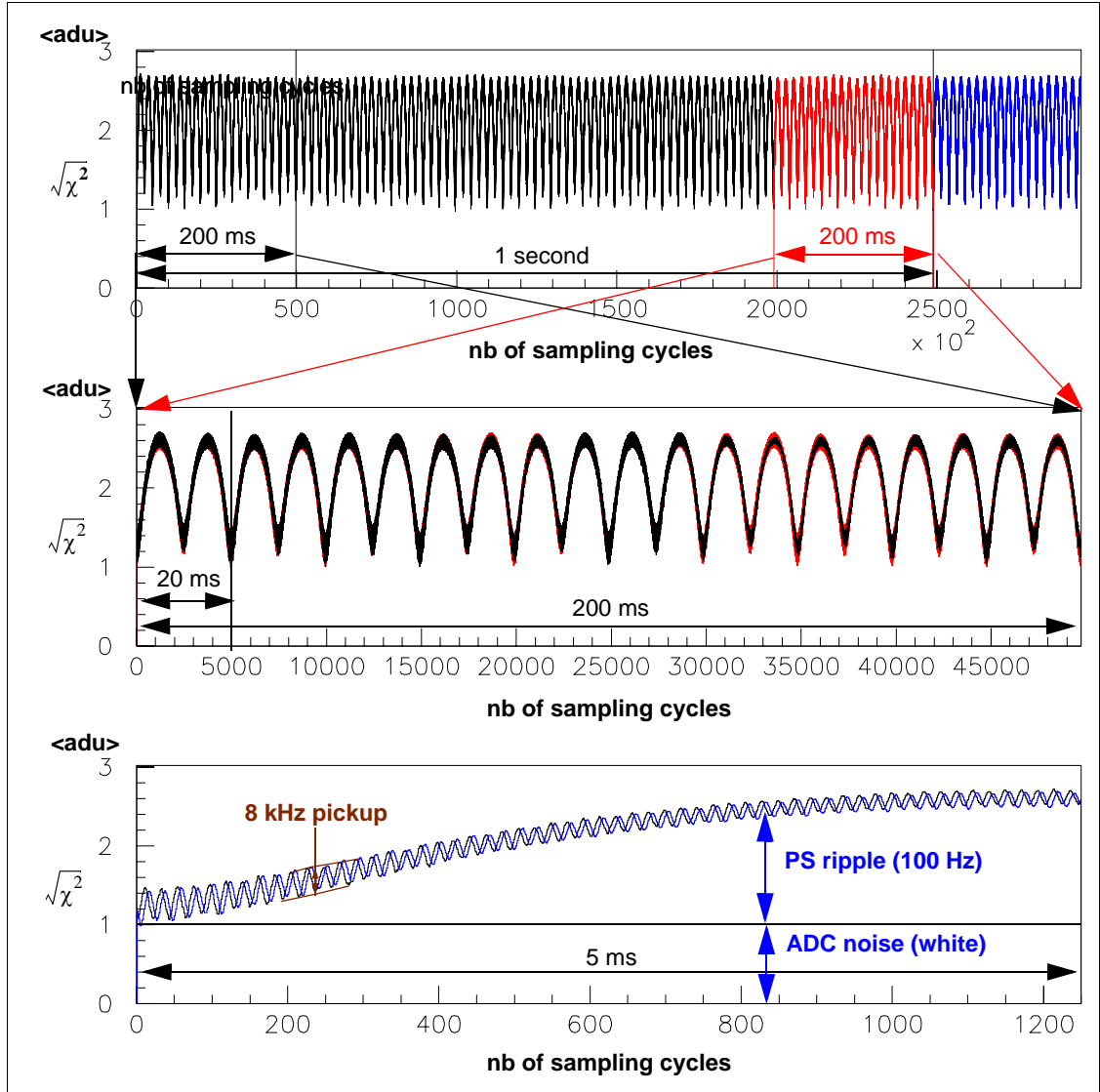
Figure 8: Constant level noise analysis using an 'auto' adaptative filter (sliding window ΔT=20 ms) which reduces white noise to 0.01 adu. The one second record of upper plot is divided in five parts. The first and the fifth parts are superimposed on the mid plot to display the phase stability of the 50-100 Hz component of the noise The identification with a line ripple yields the true digitisation frequency which is 248.7 kHz instead of 250kHz. A residual 8 kHz pickup noise is seen in lower plot (details seen in Figure 9).

the signal in a first one-cycle window with the signal in any other sliding window. A minimal χ^2 is obtained each time that the signal in the second window reproduces the signal in the first window, i.e. in case of a periodic signal for each period . This operation is expressed mathematically by the formula:

$$(1) \qquad \chi^2(k) \ = \ \sum_{i=1}^{N} \left(a_{i+k} - a_i\right)^2$$

cycle: $\Delta t \ = \ N \times \delta t$

delay: $\tau \ = \ k \times \delta t$

δt = sampling period

The end of each cycle is marked in Figure 8 by a χ^2 minimum. One counts a secondary minimum in the middle of each cycle because the ripple is almost a perfect 100 Hz signal. The precise value of the cycle length is measured using 50 line cycles, i.e. the one second interval shown in the top graph. This yields the precise estimation of the true sampling frequency to be 248.7 kHz (instead of 250) and to adjust the cycle duration in equation (1) to be N=4975 (instead of 5000). The mid graph shows the sharpness of this cycle identification owing to the suppression by a factor 100 of the random ADC noise (0.7 adu RMS) performed by the estimator of equation (1) which consists in a weighted sum of 10000 samples. However it also shows that a periodic perturbation around 8 kHz adds up to this 100 Hz ripple. This pickup is seen with a better time resolution in the lower graph. Its phase relative to the 50 Hz varies clearly from one cycle to another. More information on this 8 kHz perturbation is found in Figure 9 showing that it is not stable. We have developed tools to study this effect based on the observation that the estimator used can be understood in terms of adaptative filters. We put them aside because they are not needed at this stage.

The source of the 8 kHz noise is not yet known but it is outside our digitization system. It happens to vanish as shown in Figure 10.

3.5   Backend voltage ramps

The previous paragraph shows that each individual measurement on a time scale of a second yields a precision much better than the accuracy of the ADC which is known to be within one adu =76 µV. The question adressed by our calibration using the setup of Figure 7 is the possible effect of the connection between the signal source and the ADC. A first try has shown that the multiplexer could have a damaging effect depending on the actual values of its power supply voltages. A deviation between the values measured by the ADC and by the reference voltmeter could be the due to the voltmeter itself. The result of a manual calibration is shown in Figure 11. The end points corresponding to -32768 and 32767 digital outputs are reached at -+ 2502 mV(voltmeter readings). An offset of 0.4 mV, the same for each polarity beeing corrected, one gets the result of Figure 11. The results above -+2V are raising some questions. Remeasuring seems to yield unstable results. More investigations are needed.

3.6   Status of the seven backend channels

We have studied all seven channels multiplexed to the ADC of the CLAP backend card, following the methods exposed above in §3.2 and §3.3 (one more channel will be added in the final edition of the board : the frontend reference ground). The five channels inputs driven by frontend signal sources are loaded with a 1 K impedance. Figure 12 shows that these channels are all identically described by a gaussian white ADC noise of 0.7 adu
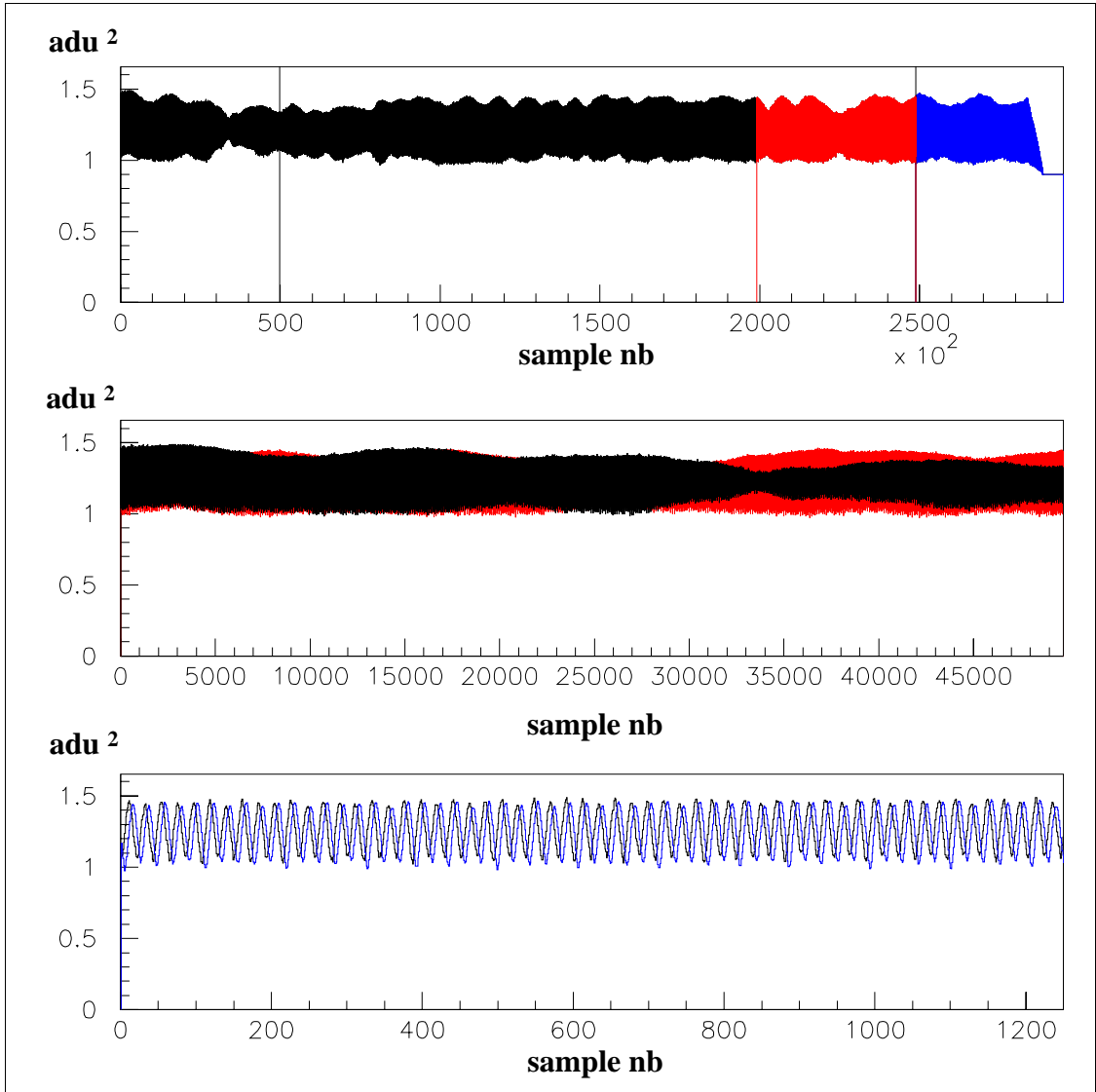
Figure 9: Pickup noise: same data as in Figure 8] but after 'quadratic subtraction' of the 50 Hz noise from the total noise. The lower plot and the mid plot superpose two records taken at a one second interval (black and red), the former plot lasting 5 ms. the latter lasting 200 ms. The upper plot lasts 1.2 second. It displays the complete sequence from the black to the red records.

(RMS). They are checked using a digital filter (the average of 100 consecutive samples) which yields a 0.07 (RMS) residual noise. The two other channels are the lemo input (#5) and the backend temperature(#4). The lemo channel has been tested either unconnected (see §3.2), or connected to a voltage source (see §3.3), or connected to a signal generator. Lastly the channel #4 showed an unstable behaviour (cf. Figure 13). It was fixed by adapting the output impedance of the thermal sensor to the input of the ADC.
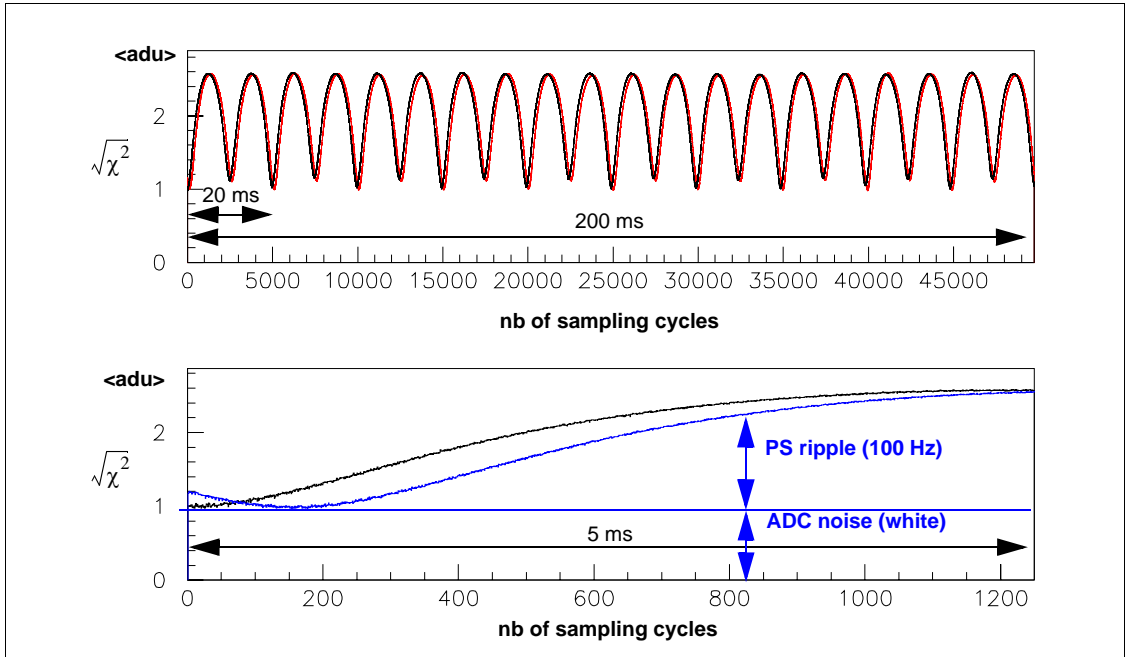
Figure 10: These data are similar to those of Figure 8, but taken an other day. The 8 kHz noise has vanished.

4 Test of the frontend ASIC using the backend digitizer

4.1 noise spectra of ULCA

The noise spectrum of the Ultra Low Current Amplifier (ULCA) in Figure 14 is dominated by a huge bump around 12 kHz which is not explained yet. This is in contradiction with the behaviour of the previous SNDICE ulca ASIC studied in ref.[1]. The filter situated between the ulca preamp and both gain 1 and gain 40 amplifiers mitigates this effect by dividing the amplitude og the 12 kHz bump by a factor 10 s shown in Figure 15.

### 4.2 linearity and calibration of ULCA

We have tested a calibration setup described in Figure 16, which turned out to be as precise as could be hoped for.

An oltronix power supply provides a 80 mV stable voltage source which is attenuated by steps down to 8 μV. This low voltage, monitored by a HP precision voltmeter, is fed on a calibrated 100 MΩ resistor to the input of the ulca and then read by the ADC through both a gain 1 and a gain 40 amplification chain.

The sampling comb provided by the attenuator using only the even value of dB counts is shown Figure 17 . This figure is used for controlling the attenuator chain and to give the impression of the sampling comb offered by this logarithmic sampling.

The calibration of the femto-ammeter is realized in two steps.

First, as shown in Figure 18, the gain 1 chain is calibrated as a function of the input voltage V_{cal} monitored by the HP precision voltmeter which is graduated in microvolt.

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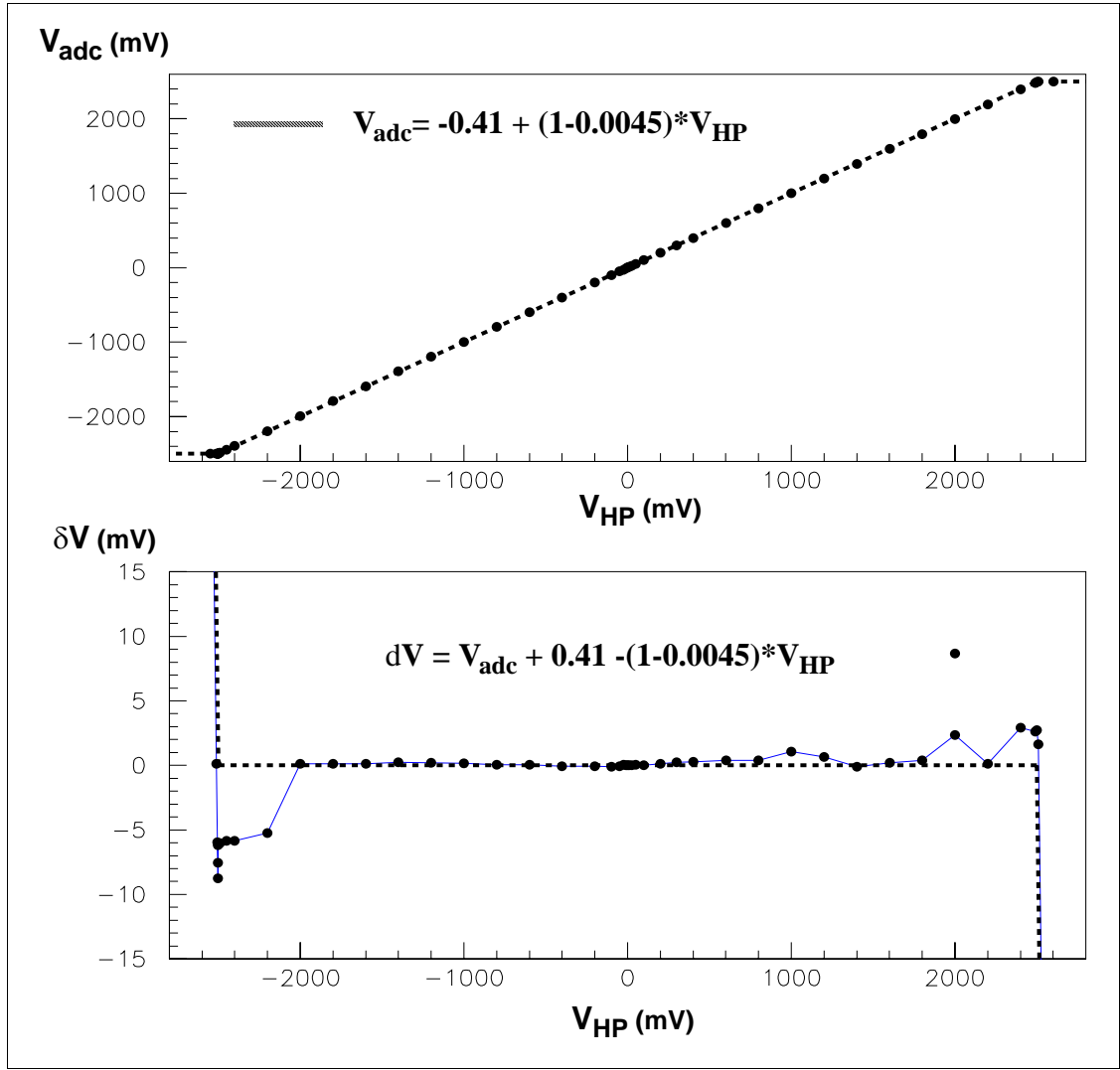
Figure 11: The ADC voltage $V_{adc}=2500*N_{adc}/32768$ ($-32768<N_{adc}<32767$) is calibrated against the reading V_{HP} of the HP voltmeter. The discrepancy between the HP voltmeter and the ADC is expressed by an offset of 0.4 mV and a relative slope of 0.45%. The outlier points are not explained yet.

The two calibration factors are the slope and the offset constant of the linear fit. The relation between the output of the preamp V_{out} and the calibration voltage V_{cal} is governed by the ratio of the calibration resistor R_c to the feedback resistor R_f and the voltage burden V_b which is the zero point of the preamplifier (all voltages beeing refered to a common input ground voltage seen by the preamplifier input):

$V_{out} = -V_{cal}*(R_f/R_c) -V_b*(1+R_f/R_c)$

At first approximation the ADC voltages V_1 and V_{40} obtained from adc counts on gain 1 and gain 40 channels as shown in Figure 11 are related to V_{out} by $V_1=V_{out}$ and $V_{40}=40*V_{out}$.

The voltage gain of the preamp is then : $R_f/R_c=124.12*2500/32768=9.4696$

This is significantly different from the nominal values of the components ($R_f=1G\Omega\pm1\%/R_c=100M\Omega\pm1\%$)

The voltage burden is consequently $V_b= 101.27*2500/32768/(1+9.4696)=0.7379$ mV
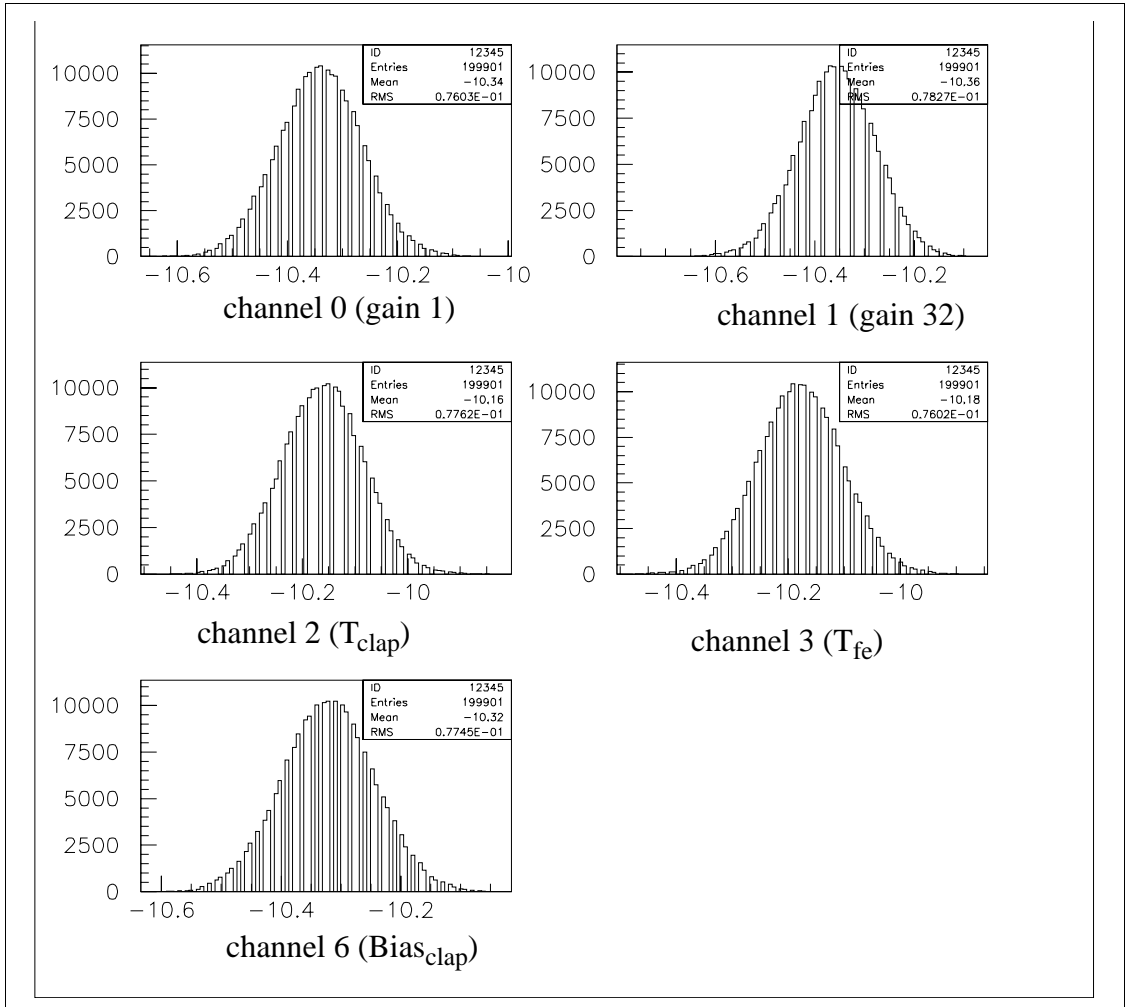
Figure 12: Digital noise measured on the five «frontend channels» when the frontend card is not connected after applying an averaging filter (mean of 100 consecutive samples). It is compatible with pure adc white noise [0.7 adu/sqrt(100)].

To be more precise one has to introduce the intermediate steps from the output of the preamp to the gain 1 and the gain 40 outputs of the frontend box and then to the ADC, the result of which is to incorporate more offset coefficients seen in Figure 11 and in Figure 19.

5   Clock adjustments

tracking of PC vs Backend clocks Figure 20

stability of 50hz pickup frequency Figure 21

connection of 50 hz phase across interrecord gaps Figure 22

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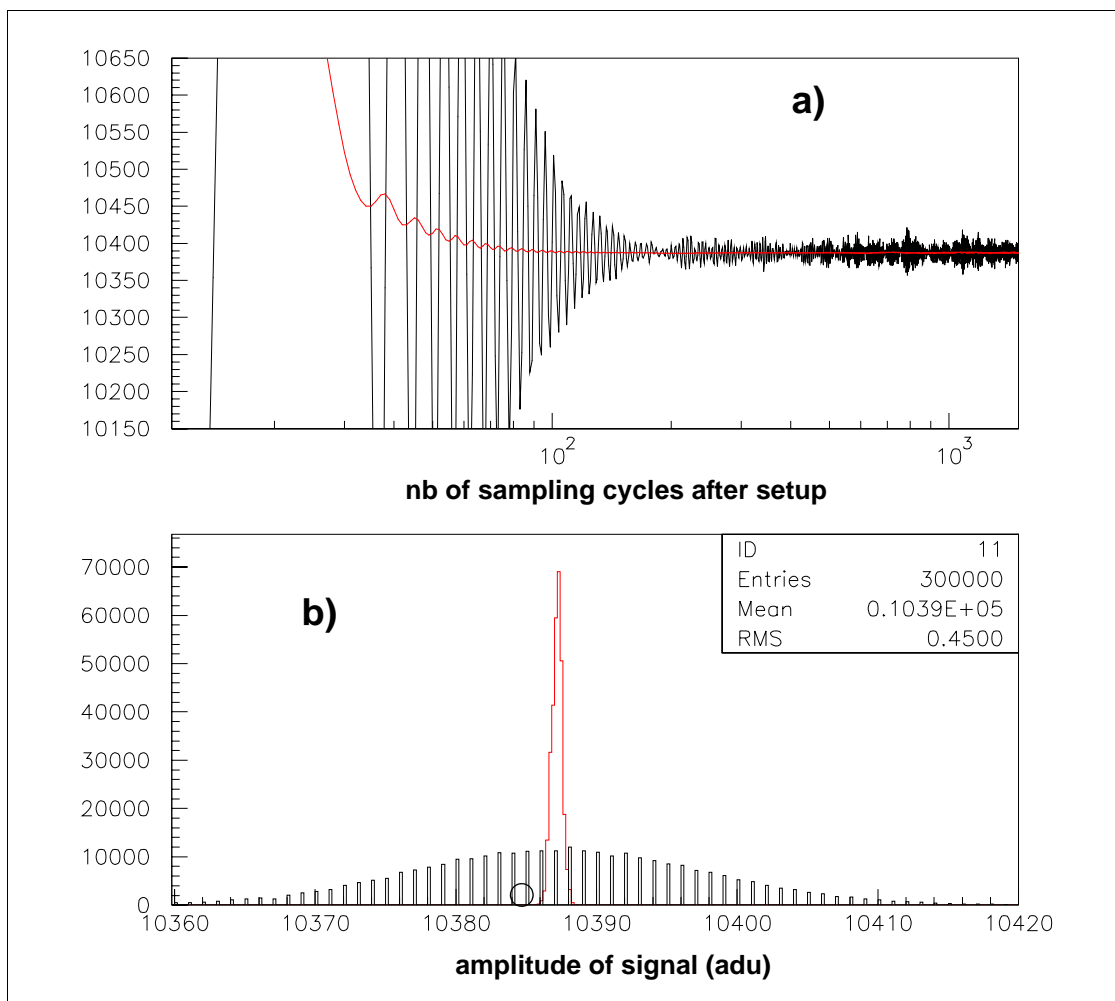
Figure 13: **a)** Channel #4 oscillate after setup; **b)** This instability yields an excess noise. The effect of a 1 kHz filter (mean of 100 consecutive samples) is shown in red and original signal in black.
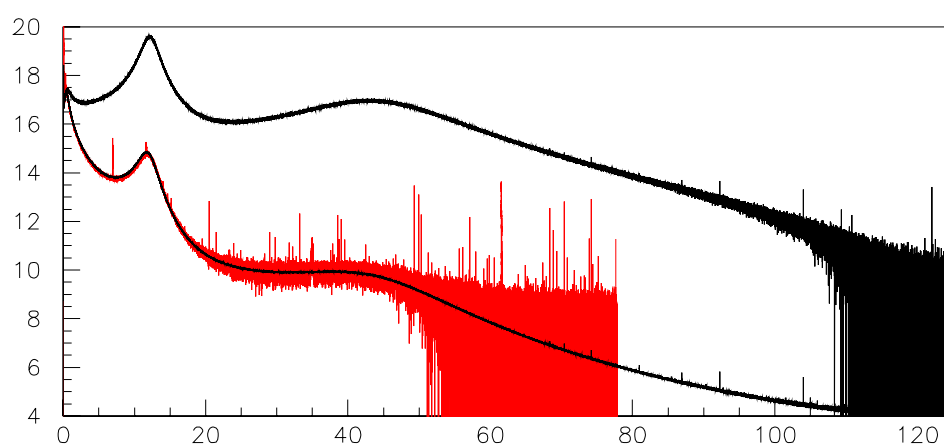
Figure 14: Picoammeter noise spectra: top preamp output spectrum; bottom gain 40 output amplifier output (in black, divided by 40) superposed with gain 1 output spectrum (in red)
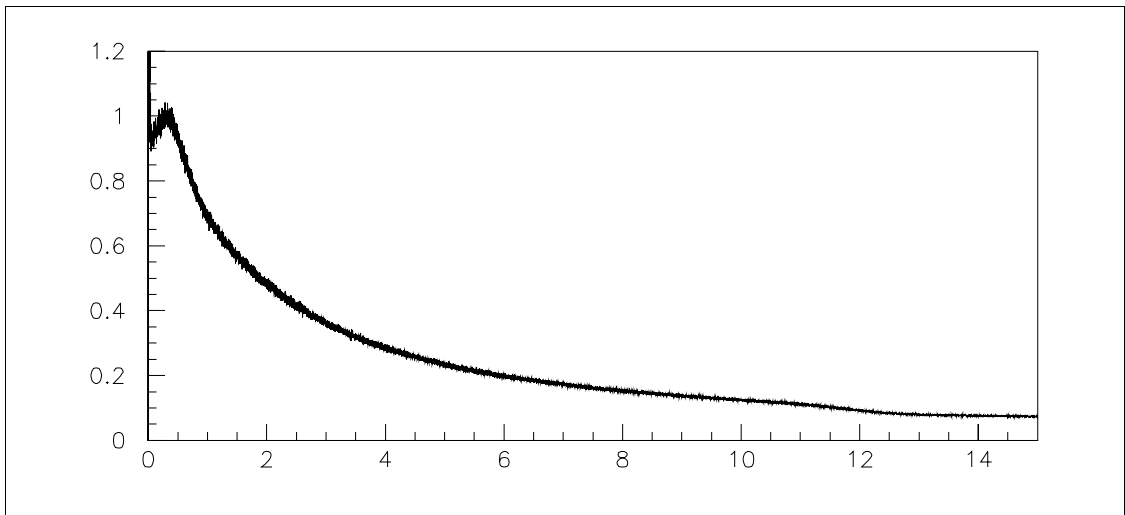
Figure 15:   Transfer function of picoammeter filter computed as the square root of gain1 output spectrum of figure 14 divided by the spectrum of preamp output in the same figure.
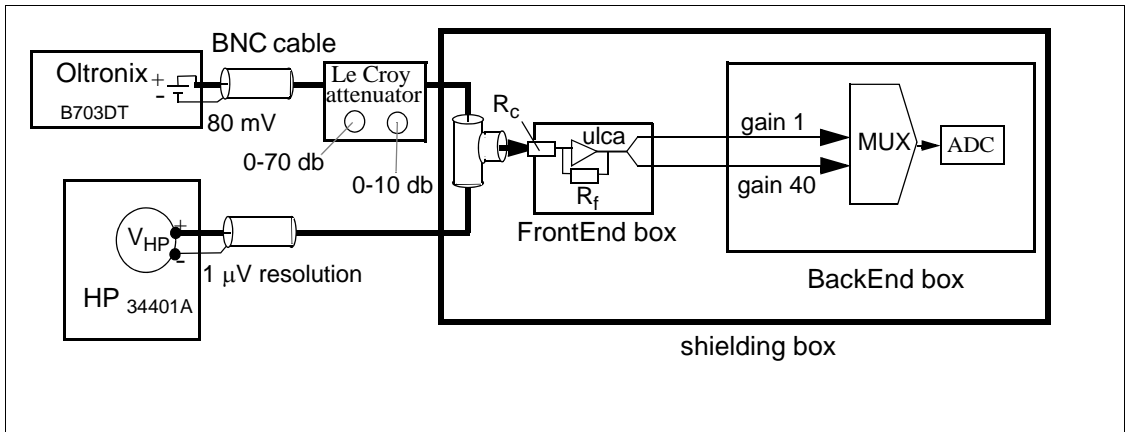
Figure 16:   Femtoammeter calibration setup. An oltronix power supply provides a 80 mV stable voltage source which is attenuated by steps down to 8 μV. This low voltage, monitored by a HP precision voltmeter, is fed on a calibrated 100 MΩ resistor to the input of the ulca.
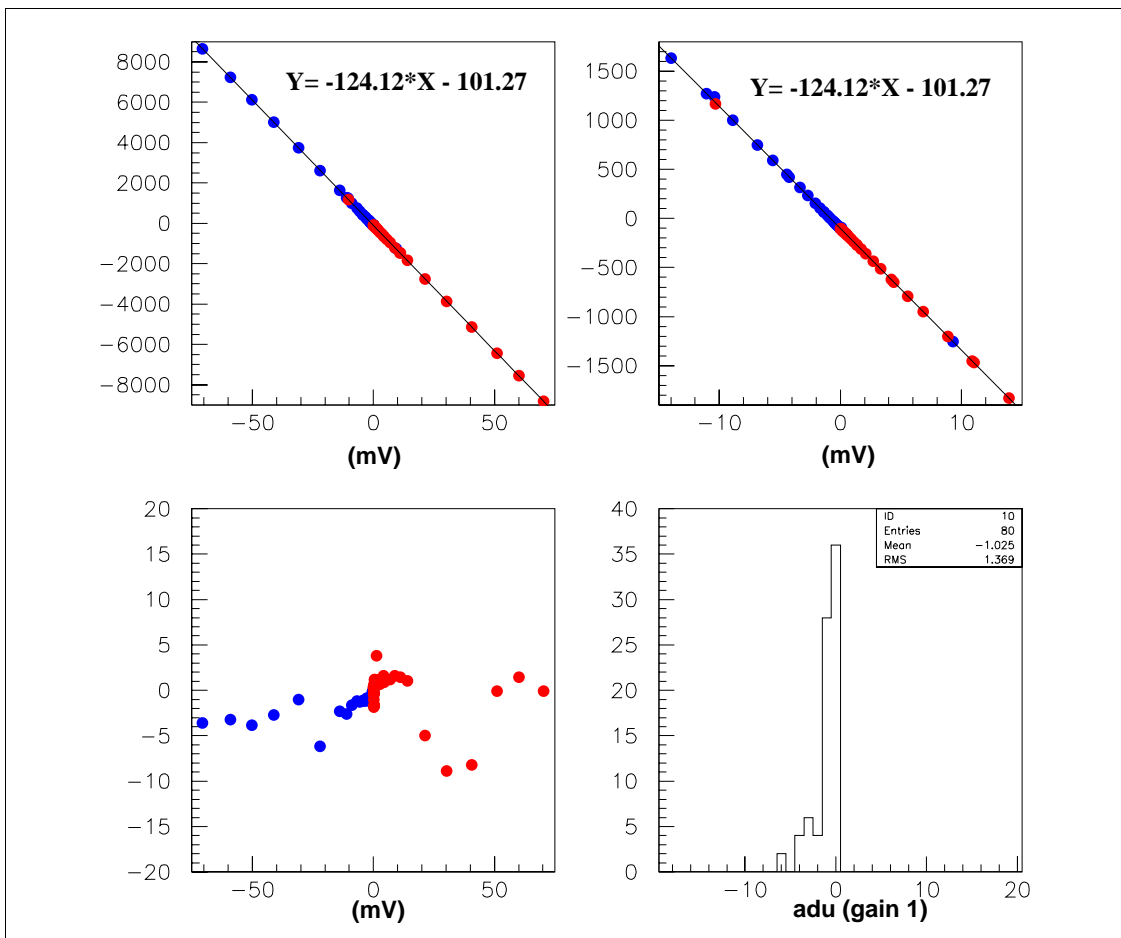
References

1. Test of a Low Current Amplifier ASIC for Cooled Large Area Photodiode, E.Barrelet et al, LPNHE 2007-4

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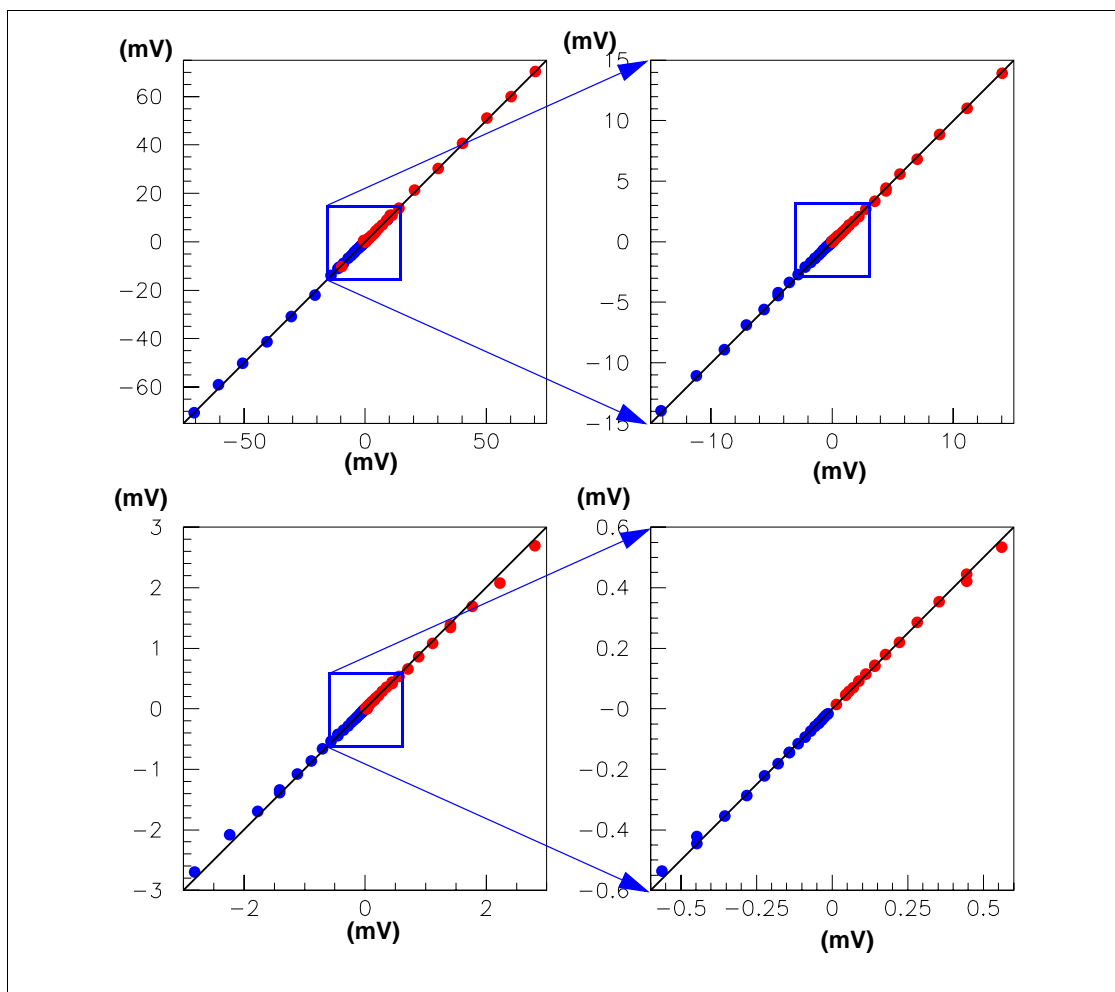
Figure 17: Logarithmic sampling of the ulca range using Le Croy attenuator. Measured values versus predicted values (test of the attenuator bridge).
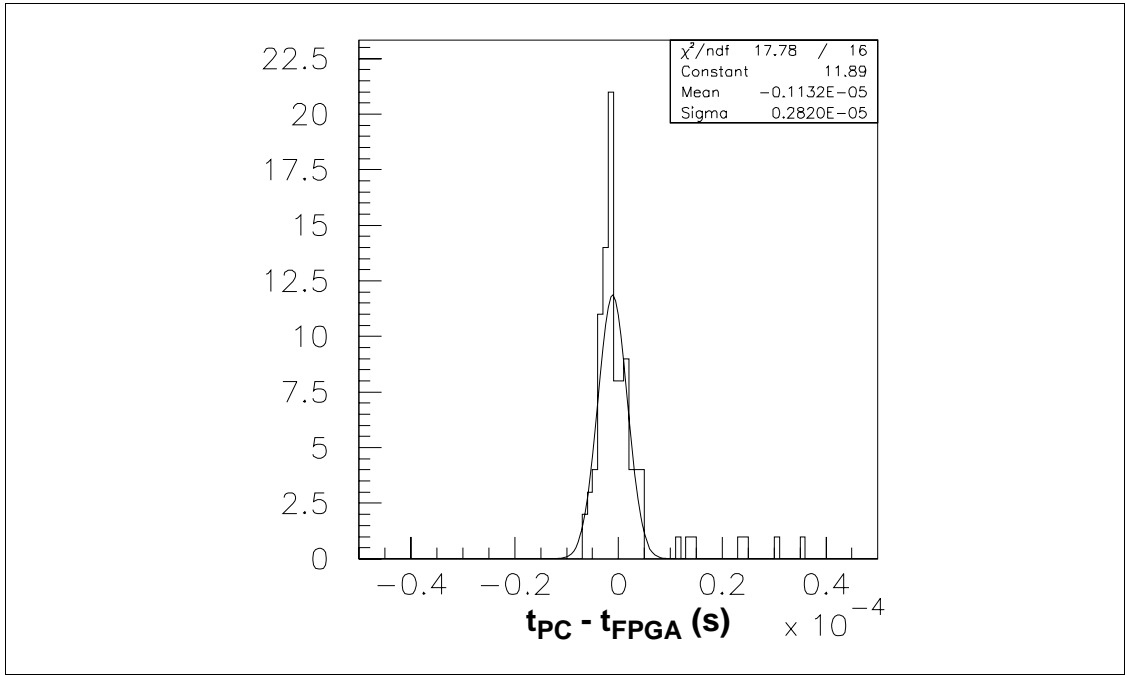
Figure 18: Calibration of the gain1 output relative to the input calibration voltage. On top the linear fit of the calibration ramp on two scales. On bottom plots the residuals and their distribution within 1.4 adu (RMS) on a range of [-8000,8000] adu
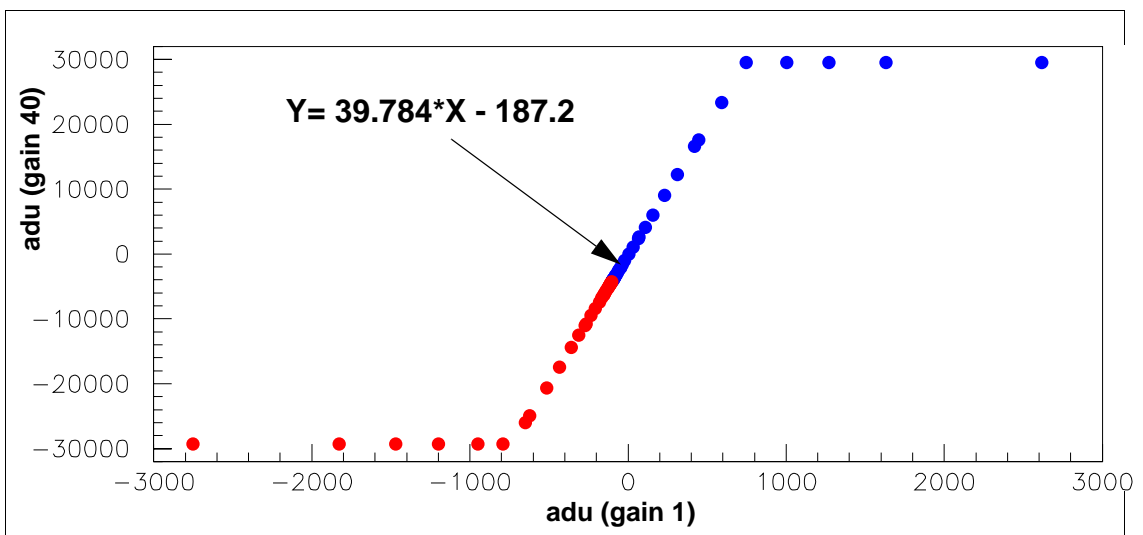
Figure 19: Calibration of high gain relative to low gain. Residuals are within 0.3 adu-gain 1 (RMS).

Figure 20: Histogram of the difference of the PC time stamp and the FPGA stamp for the same event read at the begining of each backend clap operation during a 500 second data taking. PC and CLAP backend clocks are adjusted by a quadratic formula (almost linear). Tracking precision is therefore 3μs/500s = 6*10⁻⁹ RMS. The fpga 20 ns clock period is within 2.5*10⁻⁷ of its nomimal value.
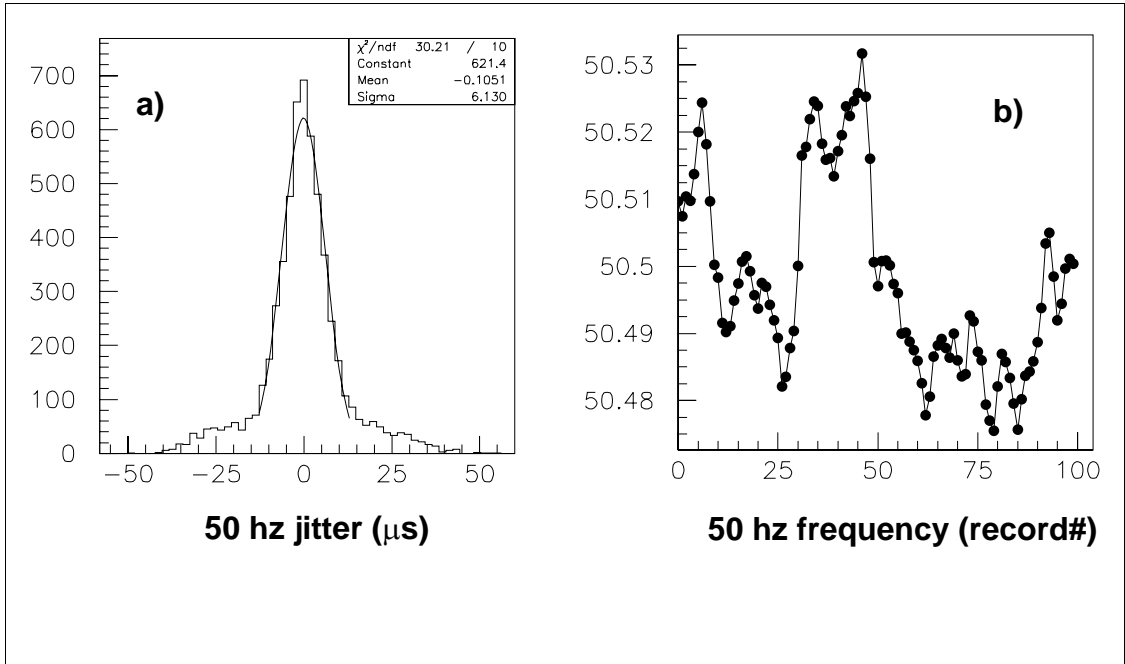
Figure 21: Stability of a 50 hz pickup signal recorded at a 500 khz rate for 100 records of 1.2 second each.
a) fluctuation of the 60 50hz tick marks around a linear fit for all records (one fit per record);
b) Fluctuation of the fitted 50 hz pickup frequency for a sequence of 100 records
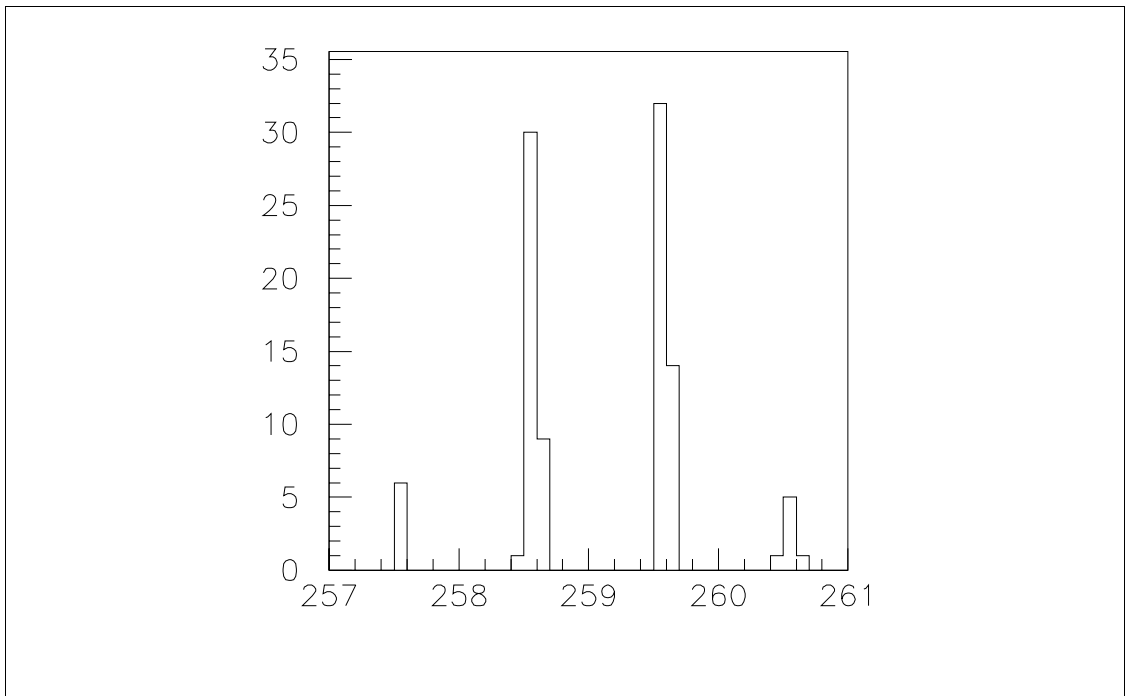
Figure 22: Phase continuity of the 50 hz pickup across the interrecord gap (lasting in average 3.9 s $\pm 1\%$). The position of the first tick mark in record n+1 with respect of the first one in record n is predicted and evaluated in tick mark units using frequency measured during record n. The splitting in four peaks is mainly due to the fluctuation of the interrecord gaps due to latency of PC system (task sharing) and to fiducial region needed for measuring the position of tick marks by the method shown in §3.4