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An Adaptable Fast & Compact DAQ for the Luminosity Measurement at HERA II

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***Abstract*— A new data acquisition system for the H1 Luminosity measurement at HERA II has been commissioned in 2002 in parallel with the machine; aiming at 1 % precision measurement on each of the 186 colliding bunches in less than 1 minute, it is based on a commercial mezzanine processing card mounted on a VME station, reading custom designed ADC & TDC VME cards via a dedicated bus. The protocol on this 20 MHz data bus is implemented on a FPGA, which also performs the triggering for 2 acquisition modes (triggered and by train), the synchronization of the digitization boards and the formatting of the data in an internal FIFO. The data are then fetched and histogrammed by a dedicated PowerPC processor. The online analysis of the distributions takes place on the VME station. Maximum histogramming rates of 0.5 MHz have been reached in the train mode (3 channels readout) and about 110 kHz in the triggered mode (26 channels readout).**

***Index Terms*— acquisition, luminosity, HERA, real-time**

I. Introduction

A major upgrade of the electron-proton collider HERA at DESY (Hamburg, Germany) has taken place in 2001. While increasing the instantaneous luminosity by a factor of 5, with a stronger focusing and bending of the electron beam[1], it also allows a longitudinal polarization of the electron beam for the H1 and ZEUS experiments recording the ep collisions. The other machine parameters remain at their pre-upgrade values: $I_{\mathrm{e}} \lesssim 30\,\mathrm{mA}$, $I_{\mathrm{p}} \lesssim 55\,\mathrm{mA}$, 220 bunches separated by $96\,\mathrm{ns}$, out of which 186 are colliding ones.

In the H1 and ZEUS experiments luminosity is determined from the flux of high energy bremsstrahlung photons emitted off the electrons at 0 degree in the field of the encountered protons. For H1 [1], the measurement of the photon's energy and impact point is performed by the Photon Detector (PD), an electromagnetic calorimeter placed in the tunnel $104\,\mathrm{m}$ from the interaction point (IP). An additional compact calorimeter, called electron tagger (e-tagger), embedded in one of the machine magnet at $6\,\mathrm{m}$ from the IP, measures the position and energy of some of the scattered electrons; it is used both for calibration and ep collision physics analysis.

The new machine set-up required the replacement of most of the components of the H1 luminosity system mainly for the following reasons:

- the *synchrotron radiation* emitted from the bended electron beam has a higher critical energy and provides dose deposits such that it called for a radiation-hard detector protected behind a Beryllium shield;
- the *repetition rate*: in the new nominal conditions, a significant signal is expected for every bunch crossing (BC) in the PD. Hence, a fast shaping is vital to avoid electronic pile-up from one bunch to the next. In its turn, it requires a precise monitoring of the signal digitization position;
- the *polarization*: with a build up time of about 20 mins, a precision on the luminosity of the order of the percent per minute on each bunch is desirable to exploit all the data.

II. Requirement of the acquisition

At high luminosity, a pile-up of the bremsstrahlung photons with a sizable energy in each BC leads to a Poissonian statistics of the number of photons and renders the previously used single photon counting method inaccurate. In addition to that, the synchrotron radiation passing through the Be shield provokes a shift of the pedestal proportional to the current of the corresponding bunch. The complete energy spectrum, including the pedestal, has thus to be exploited.

One specific difficulty arises from the high repetition rates; at high luminosity, there is a 50 % probability that a total energy above $5\,\mathrm{GeV}$ will be emitted in every colliding BC. The bunches being unequally filled, the few ones following a quiet period (e.g. empty bunches) will see the acquisition ready while the few next will be completely screened by any dead-time. This problem can only be handled by a dead-time free acquisition.

The new DAQ has been designed with the goal of reaching statistical and systematic precision of 1 % in 1 minute on each of BC, to match the polarization rise time. This requires very high statistics, unbiased energy spectrum, differentiated by types of BC (colliding, electron or protons only, empty), while the determination of the 2-dimensional distribution of the photon hit points, used to estimate the geometrical acceptance of the PD, partially masked by the beam transport elements, needs the information of all the channels.

A precision of 1 % also implies the control of the stability of the detector (photo-multiplier gains, using optical calibration events) and of the acquisition timing w.r.t. the beam clock; an offset of $1\,\mathrm{ns}$ on the peak of the signal generates a miscalibration of 1 %.

Besides the machine crew needs a fast (delay $\sim 1\,\mathrm{s}$) measure of the mean beam position and the instantaneous luminosity to perform the beam steering and to realize the luminosity tuning.

Manuscript received July 20, 2003; revised November 9, 2003.

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[1] "electron" is here used generically for both electrons and positions

Last but not least, the PD and e-tagger are also used by the physics analysis and hence should be readable by the central H1 acquisition at an average rate of 100 Hz on events completely uncorrelated to the luminosity determination.

III. The new Luminosity System

A. Detectors

Both calorimeters were completely redesigned.

1) The Photon Detector: Situated in the tunnel 104 m from the IP, in the axis of the electron beam, it receives Mrad of synchrotron radiation. Protected behind a Beryllium shielding (low Z elements scatters and stops the low energetic photons while leaving the high energy ones almost unaltered), it uses the radiation-hard technique of Quartz-fiber Cherenkov calorimetry. The fibers are oriented at 45 degree w.r.t. to the photon direction and project alternatively to the horizontal and vertical directions; they are grouped in 12 bundles in each direction and readout by photomultiplier tubes.

2) The Electron tagger: The electron tagger (e-tagger) is a SpaCal (Spaghetti Calorimeter) with scintillating fibers. It features 12 channels (2×6) in a small section ($7 \times 2.4\,\mathrm{cm}^2$) inserted in a magnet at 6 m from the IP, as close as possible to the beam line to measure the off-momenta electron deflected at small angle.

B. Analog Electronics

In the tunnel only an analog treatment is performed: at the output of the detectors 3 pre-amplifier cards drive the signals for 12 channel at a time for the 125 m long coaxial cable to the experimental area. An analog sum is also performed and a fake signal provided.

At the reception shaper boards receive the signals, subtract the fake line from all the others, removing most of the noise picked up in the cables and compensate the cable skewing in shape and amplitude. The shaped output is fed to the ADC in the form of a differential signal of up to 4 V, with a return to the base line below 1 % in less than 72 ns (see fig 1).

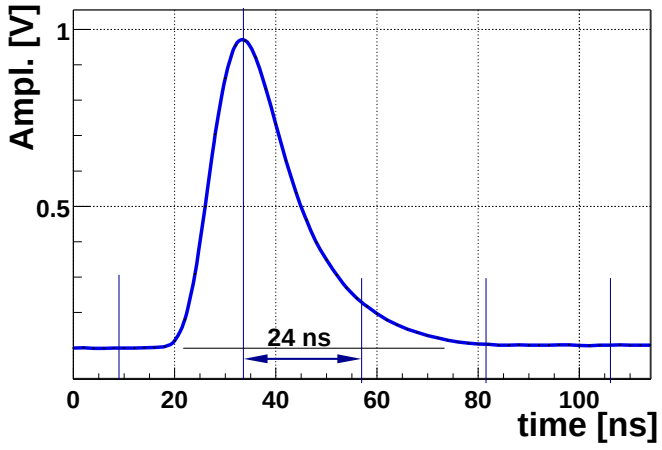

Fig. 1. Signal shape at the input of the ADC. The short red lines represent the sampling positions of the ADC. The signal goes down below 1 % in less than 72 ns (third sample after the maximum).

This fast shaping is essential to avoid the pile-up between BC.

C. Digital Electronics

The digital part of the acquisition fits in a standard 6U, 22 slot VME crate (see fig 2). It includes 6 ADC boards, a TDC board, a service module (3 slots wide) and a readout bus backplane 14 slot wide plugged on the P2 connector, all of them custom made. Commercial processor boards complete the acquisition: a FIC and a RIO 8062 VME station and a PMC format mezzanine MFCC 8441 card from C.E.S. [2]. A few slow control cards (commercial and custom) and H1 DAQ signal passing cards also fit in the crate.

One ADC board digitizes 8 signals on 12 bits at 41.6 MHz (24 ns) using an AD 9042 chip from Analog Devices and stores the samples (4 per BC) in two completely independent pipelines of a depth of 512 samples each. The one readable by VME is dedicated for the H1 central acquisition, the other is read by the custom bus, which also brings in the control lines (Pipeline Enables - PEn). Two channels are also compared to a digital threshold and provide trigger signals for each sample.

The TDC board is based on a TDC chip [3] developed for the BaBar experiment probing 16 channels by 0.5 ns steps. The measured times of up to 8 analog and 8 logical channels are fed in a pipeline readable by either of the busses.

The local (custom) bus cadenced at 20.8 MHz (48 ns) uses the J1 and J3 rows of the P2 connector (traditionally devoted to the VSB bus); 24 lines are dedicated for the data (carrying 2 samples of the ADC or 1 TDC word), 12 lines for the addresses (card, channel and pipeline index). Some control lines and clocks also transit on it.

The Service Module provides the clocks and does the phase adjustment from the main 10.4 MHz (96 ns) machine clock. It passes the H1 PEn to the ADC boards and the trigger bits to the MFCC card.

The readout sequence and bus protocol are controlled by a FPGA located on the MFCC card; the data are passed to a PowerPC processor for treatment and histogramming. About once per second the histograms are sent to the mother board (the RIO2 8062) for analysis and storage. Together with the slow control data read via the VME bus, the online luminosity numbers and position determination are broadcasted through an Ethernet connection to a remote PC.

IV. The MFCC card & code

A. Hardware

The MFCC 8441 board has originally been designed for telecoms, special protocol handling (acquisition, transmission), especially for avionics [4]. It features a Front-End (FE) FPGA Altera 10K50 connected to 64 lines on the P2 and to an equal number on the front side where space has been left for a custom electrical adaptor.

A 300 MHz 604e Motorola PowerPC processor (PPC) equipped with a 16 kB data cache arbitrates the 32 bit, 66 MHz PPC bus and provides a flexible processing power. 32 MB of RAM are accessible from the PPC, the FE FPGA and from the bridge FPGA connecting the MFCC to the PCI bus (32 bits @ 33 MHz) of the mother board in DMA mode.

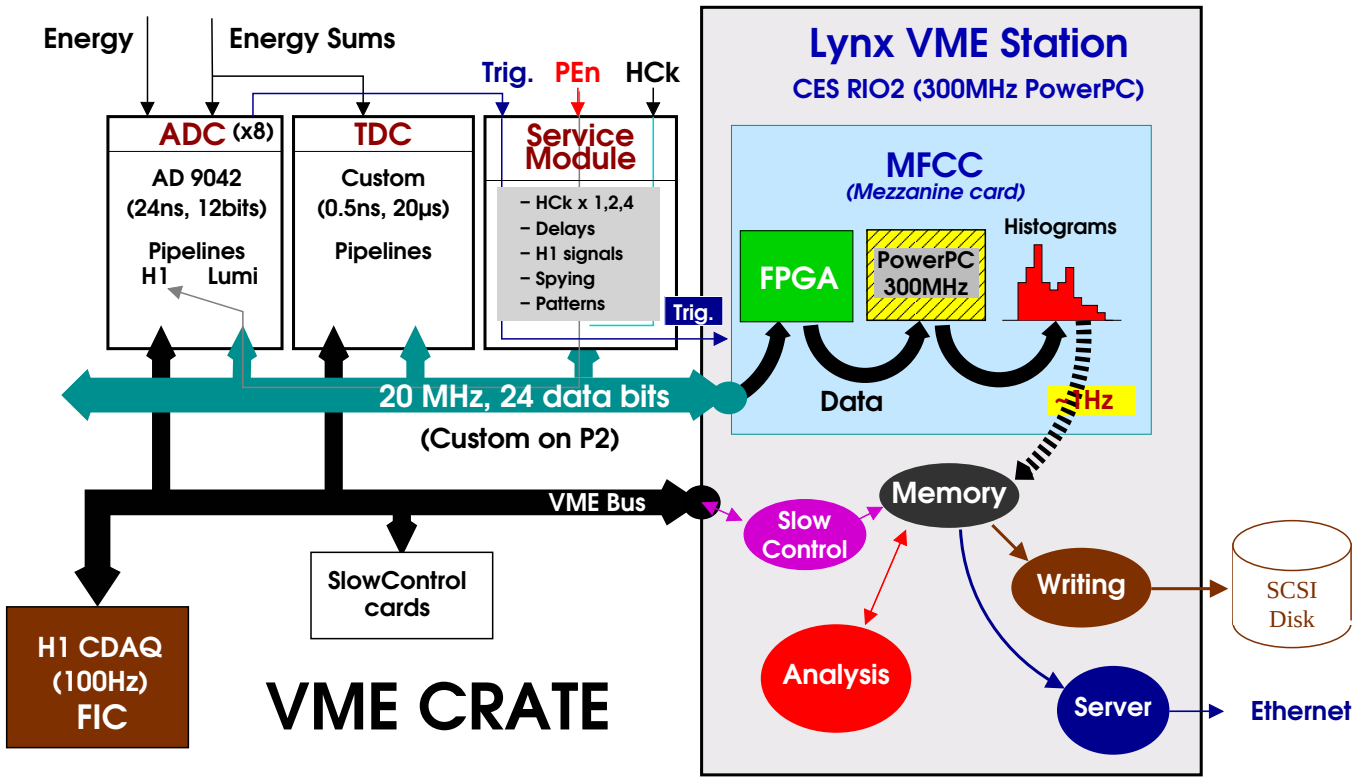

Fig. 2. Schematics of the VME crate & of the data flow in the acquisition.

B. Front-End FPGA code

The code implemented on the FPGA represents the core of the acquisition, providing the following 5 functionalities:

- a control of the acquisition modes;
- a synchronization mechanism to the machine cycle ("First Bunch" signal);
- a FIFO for the export of formatted data;
- a triggered mode for a programmable sequence of up to 32 data words. The BC number is provided in a header. Global or detailed trigger information, as well as any card/channel combination in the BC 0 (having triggered), ± 1 can be requested;
- a train mode starting on a selected BC number for a programmable length. The number of the first readout BC is written in a header, followed by the data corresponding to a programmable sequence of up to 16 card/channel addresses;

The underlying finite state machines and their interactions are sketched on figure 3 and are described below:

- a dual *trigger logic* based on
  - the 16 digital trigger bits (TB) produced by the ADC cards; the individually maskable signals are OR'ed on each BC (4 are received on each BC).
  - an internal BC counter kept in synchronization with the machine for the train mode;

  When a trigger occurs the pipelines of the ADC are stopped, a record signal sent to the TDC, the TB pattern and BC number stored. The *readout module* is then started and the trigger disabled until the readout has completed;
- a *control unit* of the ADC cards (Pipeline stop/start, synchronization);
- a *readout module* fetches the sequence of the readout (addresses of card/channels to read, length of the train) from an internal programmable memory. The sequences for each of acquisition mode (trigger or train) are independent.
  The addresses are sent and the data received on the local bus with an offset of one clock cycle to optimize the speed. The data are formatted, completed (BC number in header and if requested trigger information) and sent to the FIFO, eventually completed by dummy words to reach a total number of words multiple of 8 and allow for burst mode transfer on the PPC bus;
- a *FIFO module*, provided by C.E.S. and slightly modified, manages the 256 word output FIFO based on an internal Dual Port Memory and its interface with the 66 MHz 32 bits PPC bus, including the transfer by burst of 8 words. Every word includes a type identifier (Header, ADC, TDC or filling) and 2 bits giving the status of the FIFO (not empty, more than 8 words);
- a *User interface* (skeleton provided by C.E.S.) allowing the writing and reading of registers and parameters from the PPC bus;

C. PowerPC code

The FE FPGA itself is controlled by the PowerPC processor running a stand-alone (no OS involved) C program; the data, fetched in the FPGA FIFO via the PPC bus and through the

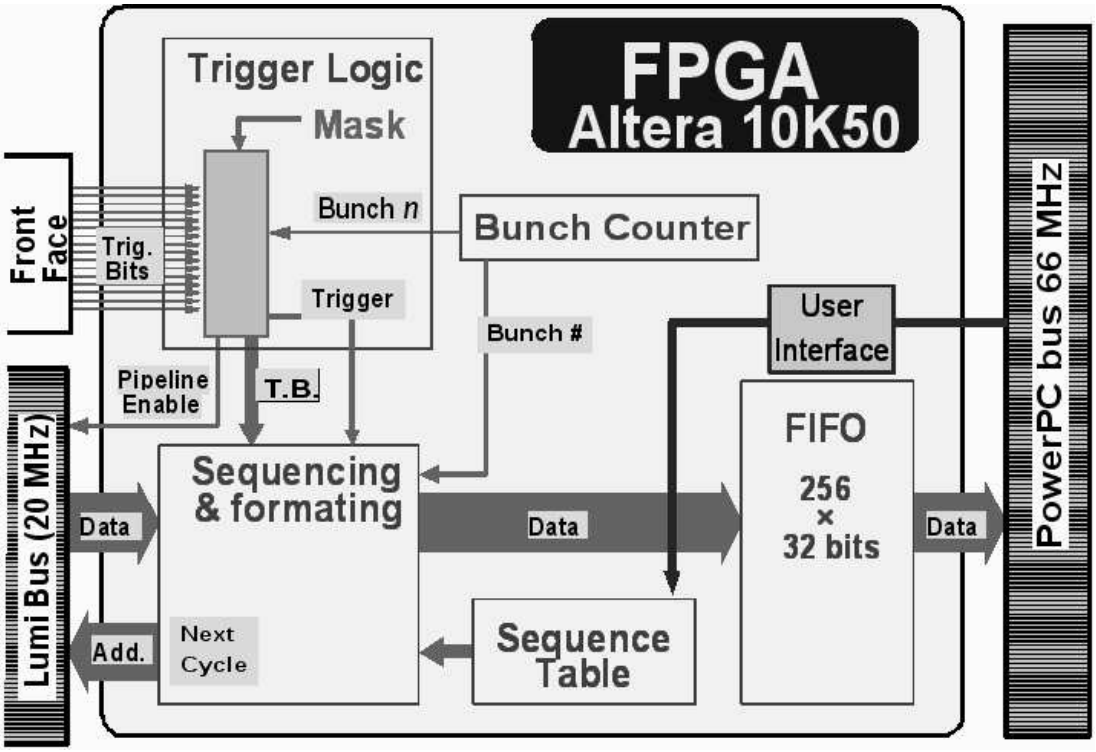

Fig. 3. Schematics of the FPGA code. See text for description.

data cache, are validated, treated and histogrammed according to the acquisition modes, BC number and type.

Different acquisition modes are used in cycles of $\sim 1\,\mathrm{s}$: in each cycle first 7000 trains of 55 BC are acquired, then about 1000 triggered events. At the end of each mode, the produced histograms are sent to the carrying board.

Every few minutes, a thousand optical calibration events are also recorded at a rate of about $1\,\mathrm{kHz}$ with the FPGA trigger mode; the sequence of addresses to read (card/channel) being different from one event to the next and known in advance, it is updated on the fly on the FPGA before every readout.

D. Performances

The acquisition and treatment time in trigger mode are of the order of $8.9\,\mu\mathrm{s/BC}$ (yielding to an observed maximum acquisition rate of $112\,\mathrm{kHz}$). Two samples (one before and one at the maximum of the signal) for 26 channels are readout: 12 PD strips and their analog sum for both the horizontal and vertical parts. The treatment implies a checking of the word type w.r.t. the readout sequence, a rejection of background events, the calculation of the mean position using the horizontal and vertical strips, and the histogramming of about 30 quantities in the RAM.

In train mode, 2 samples (same as above) from the 3 analog sums (e-tagger, PD vertical and horizontal) are readout, checked and treated. Four quantities are histogrammed according to the type of bunch (colliding, electron or proton only, empty, as deduced from the machine currents) in about $1.8\,\mu\mathrm{s}$ per BC within a train. Taking into account the overall procedure (mode setting and waiting time for the requested BC number) this time goes up to $2.0\,\mu\mathrm{s}$ per bunch when averaged on 7000 trains of 55 BC.

The acquisition limitation is completely due to the CPU speed; in train mode one BC readout takes exactly $192\,\mathrm{ns}$ on the local bus, and two consecutive BC readouts are separated by $460\,\mathrm{ns}$ (non optimized sequence rewinding in the FPGA).

The overall performances are a factor of about 2 below the theoretical value calculable from the characteristics of the hardware; a certain number of imperfections in the complex programming of the FPGA have to be corrected by the software, which itself certainly does make an optimal use of the PowerPC coding (data cache, ordering of instructions, etc). Improving the VHDL code of the FPGA would allows to simplify the PPC code, but would require new qualified manpower and a rather long time to get familiar with the inners of the VHDL code (the original author having left), only for a small benefit in terms of final statistic precision.

Would this be needed, a replacement of the MFCC 8441 by a 8843 (faster and bigger FPGA, PPC 750 @ $600\,\mathrm{MHz}$ with $256\,\mathrm{kB}$ of L2 cache, 64 bit PPC bus) would more than double - a factor of 4 seems reasonable - the performances, but again the FPGA code would need to be reprogrammed.

The performances obtained for the acquisition (see fig 4) are in the range expected; the H1 luminosity system performs well since the machine start in 2002 and has allowed to determine the online beam position and luminosity every second with the needed statistical precision ($1\,\%$) for the machine tuning. A sizable amount of work remains to be done to study all the systematics and reach the required precision offline. All the needed information is *a priori* recorded with a sufficient precision, and the flexibility of the acquisition has proven very

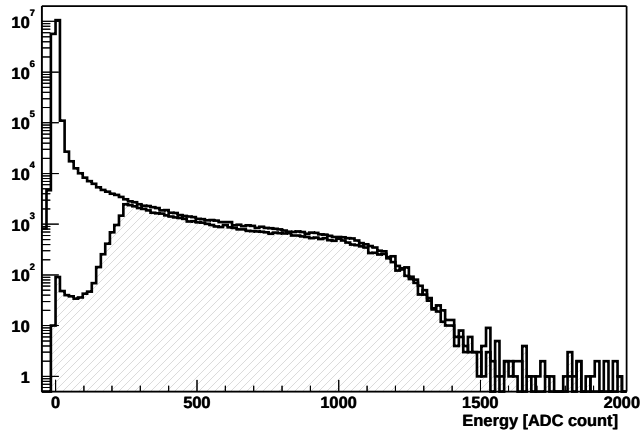

Fig. 4. Example of energy spectrum accumulated at rather low luminosity (about $0.3\,\mu\mathrm{b}^{-1}\mathrm{s}^{-1}$) during 60s in train (hollow, going down to the pedestal) and trigger mode (hatched). Their respective accumulated statistics are of 16.5 millions and about 60000 events.

valuable for example to rapidly add some histograms (at the expense of speed) in order to better control some systematics or improve the input of some calculations.

V. Upper Level Code

The board carrying the MFCC card is a RIO2 8062 produced by C.E.S.; it features a 300 MHz PowerPC processor running under LynxOS 3.0.1.

Mainly two tasks run on this board, in interaction through a shared memory:

- the acquisition: it controls the MFCC code, fetches the histograms back when they are ready, saves them to a local SCSI disk (using compressed pseudo-XML) and analyses them. It runs the analysis extracting the luminosity numbers and finally reads the VME modules for the slow control.
- the server task, which receives all the needed information (machine parameter and status, run conditions, ...) from a PC connected via TCP/IP on an Ethernet cable and sends back the online information.

Some shell scripts ensure that the two tasks are performing correctly and restart them when needed.

The analysis is due to be extended (fits on the histograms and new estimators) soon; the margin is very comfortable with only 5 % of the CPU of the board being used presently.

The PC is the only client of the RIO board; it stores the numbers in the H1 oracle database and does the interface to the outside world as a server for visualization Java applets (histograms and history).

VI. Conclusion

A complete, flexible, MHz range data acquisition setup was built and has been commissioned for the H1 Luminosity system (39 channels cadenced at 10 MHz) during the year 2002 in parallel with HERA II.

Based on custom analog and digital electronics and commercial processing cards it allowed, yet without full code optimization, typical acquisition and histogramming rates of the order of 0.5 MHz on 3 channels (analog energy sums) in a trigger-less train mode and 110 kHz on all 24+2 channels in triggered mode. A dedicated FPGA performs the triggering, readout sequencing, data reading, formatting and buffering, while a dedicated PowerPC treats the data and provides the histograms. The performances, CPU driven, fulfill the expectation in terms of statistical precision (1 % per second), while the flexibility of the acquisition permits to collect all the needed information to reduce the systematic uncertainties at the same level.

The position measurement has been working reasonably well since the restart of HERA, providing a valuable tool for the machine crew to reach the foreseen specific luminosity on a routine basis. The full performance of the machine is expected after its restart this summer (2003).

The very same electronics and DAQ are also in function for the transverse polarimeter of HERA to read 2 channels. The same hardware is now (end 2003) used for the HERA longitudinal polarimeter [5] with an independent code in the FPGA. Two channels are read in a continuous mode ($\sim$ 10 MHz) using an MFCC 8442 having an L2 cache sufficiently large to hold all the histograms.

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