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Laboratoire de Physique Nucléaire et de Hautes Energies

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Dual Gain Clamp and Sample ASIC

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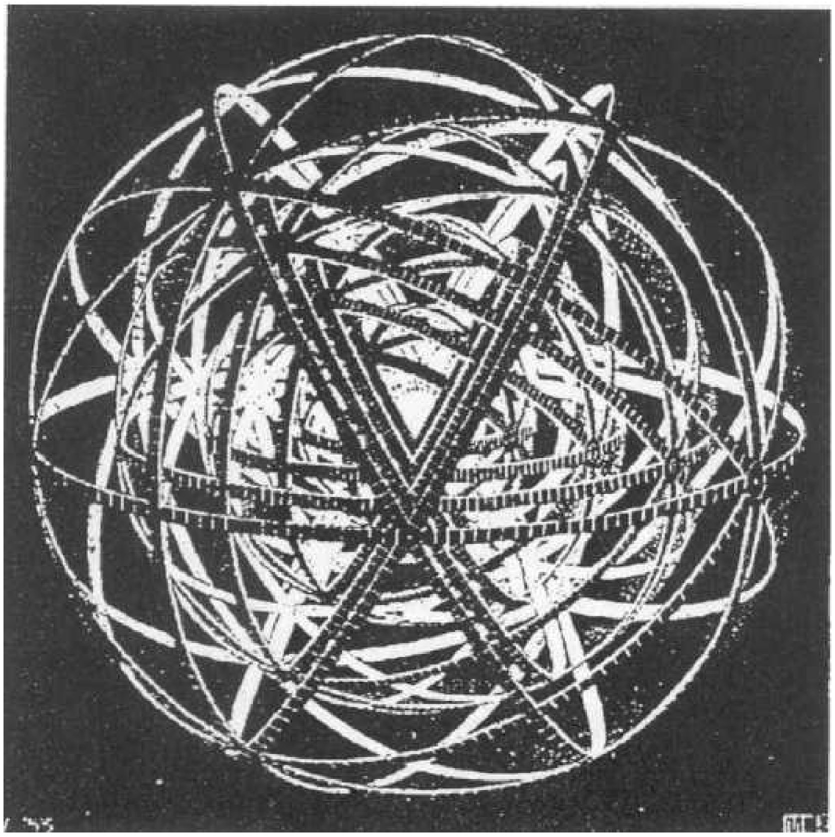

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Abstract:

This report describes the Dual Gain Clamp and Sample (DGCS) ASIC designed in LPNHE for the SNAP project, in a collaboration with Lawrence Berkeley Laboratory aiming to develop a completely integrated, space qualified, CCD readout electronics. This chip, which uses AMS 0.35 μ CMOS technology, was designed in order to optimize the first stage of a chain able to digitize a CCD output signal in the full 2 to 250,000 e^- range. It has to operate at low temperature (140 K) and to tolerate an integrated radiation dose of 100 kRad. We shall present here the electronic qualification tests, passed successfully by our ASIC. Its performances have been analyzed in the two classical modes of CCD readout, dual-integrator and clamp-and-sample, but we have pushed forward the analysis of the latter mode because we intend to use it for our next generation ASIC.

Contents

Introduction

As a first step in the design of a complete readout electronics for a Gigapixel space imager, we have integrated on a CMOS ASIC its analogical front end functions. It contains an amplification stage matching the maximum range of a CCD, say 250,000 e^-/pixel[1], with an intrinsic noise as small as the CCD thermal noise, say 2 e^-/pixel. In order to map this whole dynamical range on the input range of two 12-bit ADCs within the constraints of a low voltage CMOS technology[2], we use concurrently a gain x96 (< 8,192e^-, LSB = 2e^-) and a gain x3 (< 262,144e^-, LSB = 64e^-).

Our first section describes how this dual amplifier function is implemented in our chip, jointly with a clamp switch. Section 2 shows how we have identified clearly the origin of some gross differences between the simulations done during the design phase and the actual performances of our chip. More generally we have tried to quantify this type of discrepancies by testing the ASIC itself in addition to the transistor test patterns accompanying it. Section 3 checks the linearity of the dual amplifier using some tools designed for that application: a 20-bit calibration pulse generator and a dual 16-bit digitizer.

Following sections deal with noise studies. Section 4 describes how we tracked parasitic noise sources down to 0.02e^-, using digital signal analyzes. Section 5 shows how, within the limitations of the design kit, we have approached the simulation of the actual ASIC noise spectra. Section 6 gives a model and measures the ASIC+CCD noise performances, either in a double integrator or in a clamp and sample mode, the CCD being replaced by a resistor. Lastly section 7 and 8 report respectively the results of radiation and of cooling tests checking the compatibility of AMS 0.35μ technology with the generic mission specifications.

Two further developments have been undertaken: the integration of our ASIC in our CCD and in our IR pixel test benches. They will be the subjects of two other reports.

[1] Conventionally $1\,e^- \leftrightarrow 4\,\mu V$

[2] Output swing is set to 3.1 V, but AMS 0.35μ technology supports a larger range.

1 Description of the Dual Gain Clamp and Sample amplifier

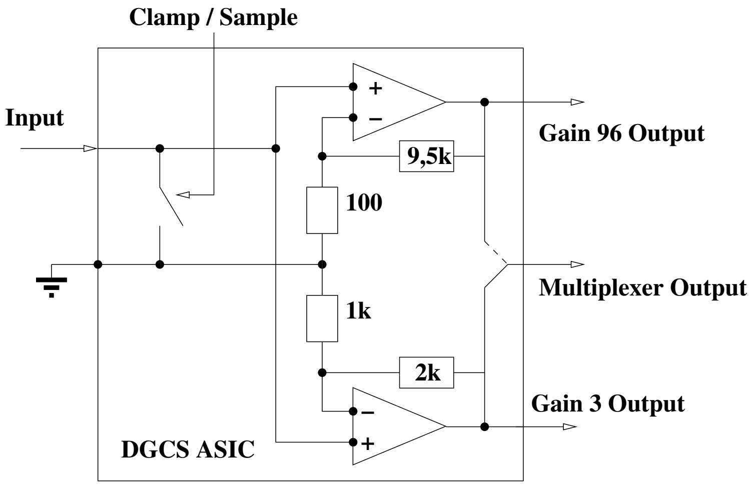

Figure 1: *Main components of the Dual Gain Clamp and Sample (DGCS) ASIC.*

1.1 Specifications of the ASIC chip

The general principle of the DGCS amplifier is shown in fig. 1, and detailed schematics can be found in appendix A. An individual chip holds four DGCS amplifiers, in addition to six types of test transistor patterns (200×0.5, 10×0.5, and 10×10 μm, both PMOS and NMOS). The layout was submitted in August 2003, the chips were received in November 2003. The tests were carried out from January to October 2004.

The DGCS amplifier is designed to work as part of a readout chain, at the output of the follower amplifier, which is built inside the detector. The input resistor can vary from 500 Ω (EEV CCD) to 10 kΩ (IR pixel detector). We can also choose whether to include a link capacitor or not (AC or DC mode).

AMS 0.35μ technology is limited to a 5 V total range; the original intent was to use a bipolar range from +1.5 to -3.5 V, -3.5 V corresponding to a pixel well capacity of 290,000 e^- for a gain 3 amplifier. We chose to use a symmetrical +2.5 to -2.5 V range instead, allowing to work with both types of CCD substrates, and a maximum well content of 208,000 e^- or holes.

Other specifications include the limit on the power consumption of an amplifier, which was set to 1.5 mW, the possibility to operate at temperatures as low as 140 K (the design kit does not go lower than 230 K) and a resistance to radiations up to 100 kRad.

1.2 Dual Gain principle

Let us recall the usual context of a dual gain chain. The detector signal is quantified ($k\,N_e$ where k is the "one electron" signal). Its Poisson noise $k\sqrt{N_e}$ adds up quadratically to the ADC quantization noise $LSB/\sqrt{12}$. The corresponding noise increase is $(LSB/k)^2/(24\,N_e)$.

Taking the same numbers as above, at the top of the high gain range, the low gain LSB/k is $64\,e^-$ and N_e is $8192\,e^-$. Therefore passing from the x96 to the x3 ADC yields a negligible increase of the noise (2%, barely seen on a peaked luminosity distribution and not seen at all on a continuum). However a good engineering practice consists in aligning high gain and low gain digitized data within one high gain LSB, in order to avoid missing or overlapping codes. This requires a 0.02% precision.

1.3 Clamp and sample principle

A typical CCD has a DC offset up to 10 V or more, whereas the gain 96 input range is less than 40 mV. As a consequence, the CCD is coupled to the amplifier through an external capacitor. An on-chip clamp accomplishes the necessary DC restoring. For the DGCS chip the aim is to achieve a DC restoring synchronized with the reference level of the CCD with such a precision that the classical Correlated Double Sampling (CDS) function is not needed anymore. This principle is used by the Megacam CCD readout chain, which is a remarkably simple and robust "one-clock" system. This system is particularly recommended when all the electronics are near the CCD, because ground to ground variation occurring between the clamping phase and the sampling phase will not affect the signal.

2 Investigation of the problems of the DGCS ASIC

The high gain[3] channel has a gain of approximately 60 instead of 96 and an offset around - 600 mV. We managed to reproduce those problems in simulation, to confirm the underlying explanation by measures on a key transistor, and to understand how those defaults escaped the design software.

2.1 Identification of the problem in the layout

The decrease of gain and the offset were reproduced in the simulator by adding parasitic resistors in several key connections (see fig. 2, and annex B for the simula-

[3] Usually it will be referred to as ‘gain x60’ in order to avoid misunderstandings, as noise figures are depending on the real gain.

tion results). The parasitic resistor between the ASIC theoretical ground point and the actual ground pad accounts for the decrease of gain, by modifying the bridge resistor values. On the other hand, the first stage of the amplifier includes two matched current sources that were supposed to subtract the same amount of current *I* to the input transistor currents *I+* and *I-*; the parasitic resistors on their grid voltage inputs create an asymmetry, accounting for the offset.

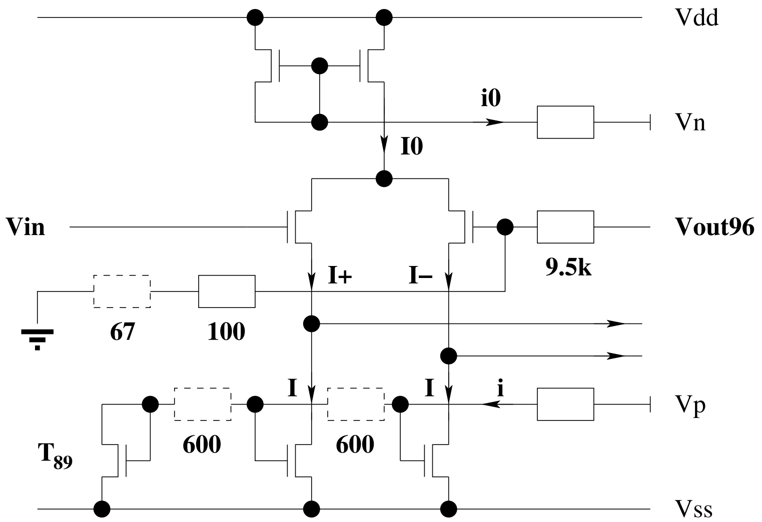

Figure 2: *Schematics of the first stage of the high gain channel of the amplifier showing the parasitic resistors affecting the performances in dotted lines. The 67 Ω resistor changes the V_{out96}/V_{in} gain ; the two 600 Ω resistors cause the imbalance in the subtracted current I, leading to an offset.*

2.2 Experimental confirmation

On the experimental side, the existence of such parasitic resistors was proved with by measuring the current-voltage curve on one transistor of the current mirror (T_{89} on the schematics Figure 2). The plots on Figure 3 show the large difference between the simulated and experimental current-voltage characteristics, and the linearity of the voltage difference as a function of the current. This matches what one would expect with a large access resistor (around 1660 Ω according to this measure, comparable to the total of 1200 Ω used in the simulation) between the voltage measurement pad and the transistor. We can note that this effect appears also on the test transistors included on the chip (graphs on Figure 4), but is nowhere near as important.

2.3 Origin: design package

The origin of this problem lies in the design of the chip: the paths to the ground pad and to the affected voltage supply are excessively convoluted, to the point that the

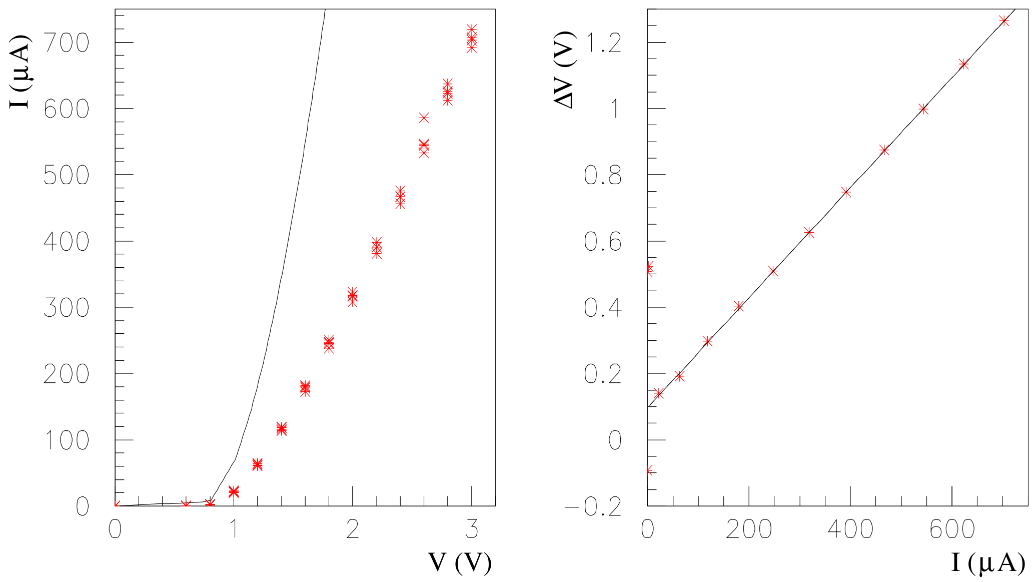

Figure 3: *a) Comparison between the simulated (line) and measured (four series of points) current-voltage characteristics of transistor T_{89} (cf. previous figure). b) The linear fitting of the voltage difference as a function of current (for one transistor) gives a value of 1660 Ω for the parasitic access resistor.*

values of the parasitic resistors adopted for the simulation are well in line with their actual geometries. This error could not be detected by the design software, since the AMS 0.35 μm package used for this chip does not take parasitic resistors into account, contrarily to the previous one used by our team (a 0.6 μm package).

2.4 Consequences for noise measurements

Besides the change in gain and the important offset of the high gain channel, this problem has other consequences affecting the noise analysis measurements. On both channels, there is a shift in pedestal between clamping and an input of zero. The output during clamping is equivalent to an input of -1 mV on both channel, and can be explained by a section of the grounding parasitic resistor situated between the clamp 'grounding' point and the actual ground pad (see next part for details). Additionally, the matched current sources problem increases strongly the sensitivity of the offset to the power supply voltage: up to 0.2 mV offset variation instead of a projected 5 μV for a 1 mV variation of the supply, on the high gain channel. At its worst, power supply drift created a 5 μV drift in pedestal level during a data acquisition run, exceeding the level of noise we aimed at measuring.

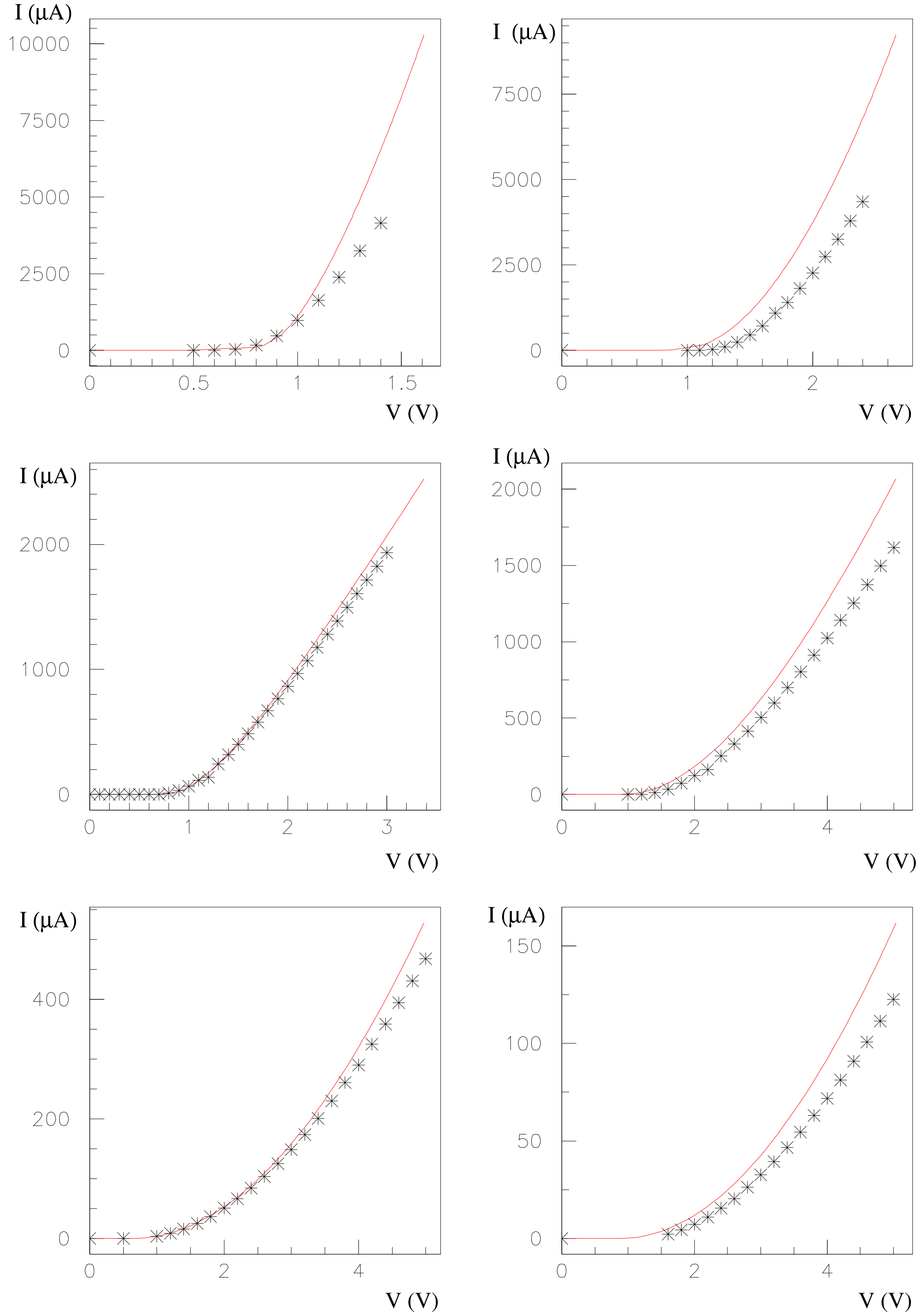

Figure 4: *Left: Comparison between the simulated (line) and measured (points) current-voltage characteristics of the control transistors of the chip. Left column: NMOS transistors, right: PMOS (with* I_{DS} *and* V_{DS} *polarities inverted for ease of comparison). Top to bottom: dimensions* 200×0.5, 10×0.5, *and* 10×10 μm.

3 Linearity of the amplifiers

3.1 Test hardware

The tests of linearity in 'DC' mode (in fact pulses lasting around one millisecond) are part of the performance assessment of the ASIC, and also a way to explore some of the possibilities offered by our pulse generator and digitizer/readout system. The former is a 20-bit pulse generator, switching between the output of a 20-bit Digital-Analog Converter and a well-defined reference (ground), with an output ranging from -2.7 to +2.7 V. The latter includes two 16-bit Analog to Digital Converters working on a range of -2.5 to +2.5 V (giving an LSB of 76 μV). Both were constructed at LPNHE. On the 'convert' trigger, both 16-bit ADC outputs are stored by a 32-bit frame-grabber, with a transfer rate of up to 20 MHz (National Instruments NI 6534).

3.2 Data acquisition

The protocol for linearity measurement is straightforward thanks to our integrated Labview program: first a DAC ramp is input through the pulse generator on both inputs in the dual 16-bit digitizer, with the chosen range, step and number of repetitions at each value; then the ASIC is inserted and the same ramp is applied as ASIC input, while the ADCs measure both ASIC outputs. With the averaging, we obtain a RMS of 0.21 LSB (16 μV) on a 16-bit ADC for the low gain and 2 LSB for the high gain (153 μV), which is far more sensitive to input noise.

The power supply voltages fixing the ASIC output range were chosen to fit the $\pm 2.5\ V$ range of the ADCs. It was also verified that changing the bipolar range (e.g. -3.5 to 1.5 V) did not affect linearity in the measurable part of that range.

3.3 ADC to voltage conversion

The two ADCs give out slightly different numerical values for the same input, as illustrated Figure 5. This is explained by differences of a few millivolts in the real ranges of the ADCs. This effect is correctly suppressed by the ADC-to-voltage calibration, as seen on the second plot on the same figure. Since the ASIC is designed to work with 12-bit ADCs (LSB = 1.2 mV), the level of the residuals is quite acceptable. On a side note, the uncertainty (around 0.5 mV) on the offset of the ADC-to-voltage conversion can affect the offset measurements, translating into an error of up to 30 mV when calculating the high gain offset.

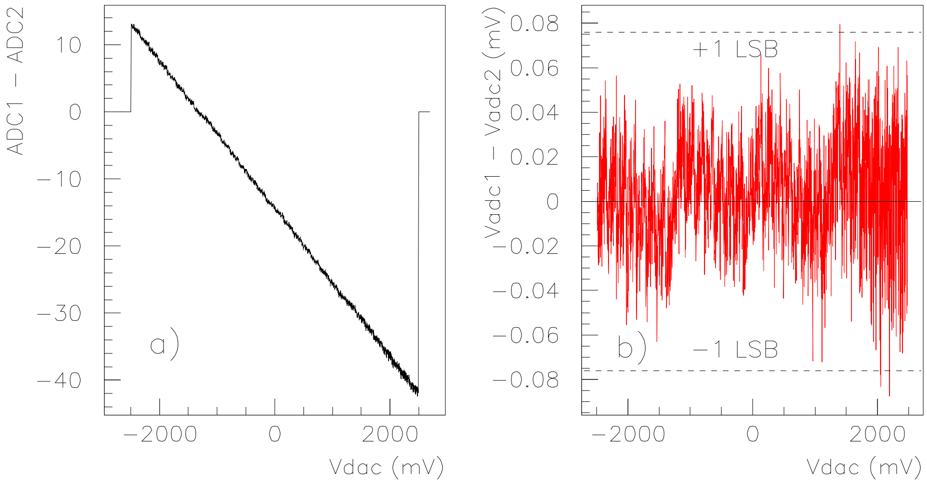

Figure 5: *Comparison of the two 16-bit digitizer channels using: a)the difference of the two integral linearity characteristics (ADC vs DAC) which displays a 0.1% relative difference of slope, b)the difference of the two differential nonlinearities (residuals of a linear fit) which remains below ±1 LSB (16-bit ADC).*

3.4 Linear fits

The linear fits on the non-saturated parts of the response curves (Figure 6) give respectively:

- For the low gain channel: a gain of 2.98 and an offset of 5.3 mV
- For the high gain channel: a gain of 57.9 and an offset of -575 mV

In the case of the high gain amplifier, the residuals show digitization patterns that can be generated by fluctuations in the DAC or in the ASIC offset; no deviation from linearity can be attributed to the amplifier. However, in the case of the low gain, there is a clear pattern in the deviation from the linear fit. A partial fit on each branch of that pattern shows a gain of 2.97 in the negative part, 2.98 in the positive part and only 2.75 in the central part of the $\pm 2.5\ V$ interval. The next paragraph explains this pattern and how to eliminate it to obtain the true gain.

3.5 Effects of the parasitic resistor on the linearity measure

The different segments of the low gain residuals match exactly the different modes of the high gain channel. We explain the apparent break in linearity by a coupling through the grounding parasitic resistor discussed in the previous part. With a resistance between the point where the resistor bridges of both gains are joined and the

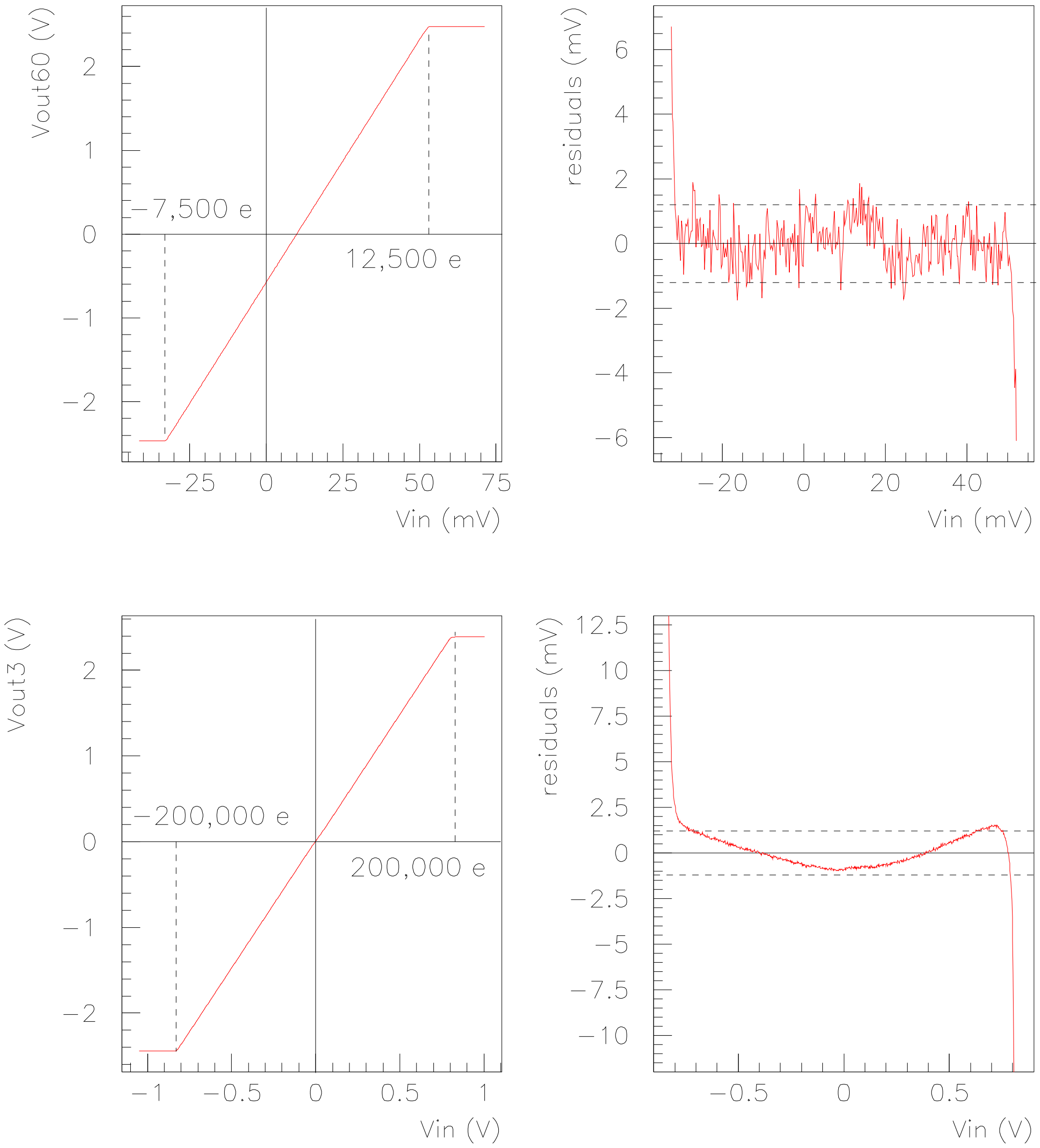

Figure 6: *Results of linearity measurements for high and low gains (respectively top and bottom graphs): DC transfer functions (left) and residuals after linear fitting (right), compared to a 12-bit ADC LSB (dashed lines).*

ground pad (see Figure 7), each output creates an additional voltage on the feedback input of the other amplifier.

The shape of the low gain residual graph is reproduced by simulating such a configuration. To eliminate this coupling effect from our data and look at how the amplifier would work without those parasitic resistors, we calculate a 'parasitic voltage', created by the current coming from the high gain resistor bridge through a part of the parasitic resistor. Then we calculate the effective input and output voltages by subtracting this parasitic voltage to the measured inputs and outputs. With a common resistor of 19 Ω, out of a total 67 Ω on the high gain channel, this operation effectively eliminates the pattern due to coupling (see the residuals after correction in Figure 6). The remaining non-linearity is less than 0.1% of the output range. This shows that eliminating the parasitic resistor should bring the residuals down to a reasonable level compared to the 12-bit ADC that will be used for the integration into a readout chain.

3.6 Anatomy of the parasitic resistor

To complete this picture of the grounding parasitic resistor problems, we can now evaluate what creates a voltage shift during clamping (see Figure 7). The high gain channel has then an output of -635 mV ; by comparison the low gain channel output is negligible. We can compute the voltage at the bridge junction on the 19 Ω resistor ($V_j = -1.25$ mV), and deduce the section of the 19 Ω resistor that must be between the clamp switch and the ground pad to have a -1 mV input: $R_{clamp} = 15\,\Omega$.

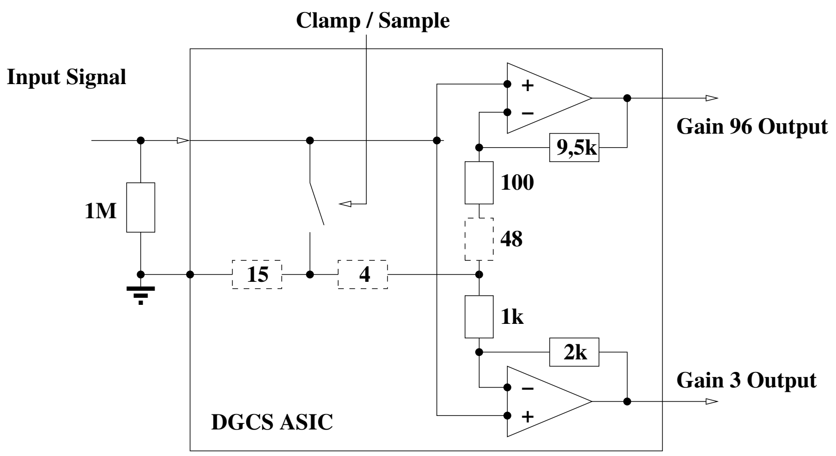

Figure 7: *Positions of the parasitic resistors (dotted lines) on the path to the grounding pad.*

4 Noise study without CCD: Experimental Method

The main cost when going from a state of the art op-amp [4] to a CMOS amp is the degradation of noise performances coming with a power reduction. This drawback is quantified (6 instead of 4.5 $nV/\sqrt{Hz}$) and balanced with the advantages of CMOS: possible low temperature operation and integration of the full digitization chain.

The other cost of CMOS integration, the limited dynamical range, is canceled in our application by the double gain feature which takes advantage of the "Poisson" noise dominance in the low gain range (cf.linearity study).

Another point deserves attention: the clamping which is done at the common input of the two amplifier channels. It provides both the "DC restore" and the "zero" function (suppressing for both channels the "$\sqrt{kTC}$" charge resulting from the CCD reset). This preserves the attractive "one clock" feature of the Megacam scheme. However the "clamping noise" is amplified as much as the signal. We have to check that it does not ruin the overall noise figure.

Our goal is: first to measure and characterize each noise component, second to check our measurement against the theory and third to check it against the result of the AMS 0.35μ simulation kit.

4.1 Target noise level

Our target is a RMS noise figure of $2e^-$, i.e. about 8 μV. Therefore we have to measure noise components in the 1 to 4 μV range and check the sensitivity of these components to external factors within 10%. For this reason we ask a noise measurement with an absolute precision of 1 μV (RMS) and a relative precision of 0.1 μV. This is rather delicate, mainly due to the fact that you cannot "see" an external noise source below the level of your thermal noise unless you guess that it is there.

4.2 Input circuit

The noise study presented here was just done at "pedestal level", using a set of resistors to simulate the output of the CCD detector, as seen Figure 8 ($R_{CCD} = 500\,\Omega$ for EEV and $R_{CCD} = 2\,k\Omega$ for LBNL). The amplifier was tested either in a "DC mode" or "AC mode" (i.e. connecting the R_{CCD} to the amplifier input through a link capacitor C_l, fixed to 1 nF in Megacam). In both case the presence of R_{CCD} is essential for the clamping.

The reason why we have not extended this study noise at various signal amplitudes

[4] UCSD controller uses AD 829 and Megacam OPA 627 (best noise figure $\approx 4.5\,nV/\sqrt{Hz}$, swing $\pm 15\,V$).

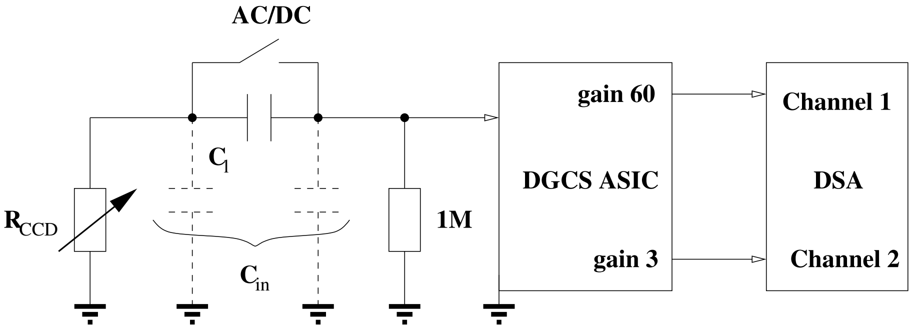

Figure 8: *Electrical setup for DGCS ASIC noise test.*

comes from the lack of a sufficiently low noise generator. All generators tested on this purpose being too noisy by orders of magnitude, we built one. The intrinsic noise of this homemade generator is negligible compared to our ASIC, but it presents a slow drift of about 5 μV, which made it unfit for the following study.

4.3 Waveform recording

Digital signal processing permits to measure noise spectra and to emulate any type of filter. For example, when we emulate a perfect integrator, i.e. when we compute the sum of all samples within a given time window, we can vary the length of this window from a fraction of a microsecond to a millisecond, which is totally impossible with an analog integrator. Practically, as we do signal processing offline, in order to keep data volume and readout time in reasonable limits we have defined three types of windows each containing 10^4 samples as shown in Table 1.

Table 1: *The three types of waveform recording.*

waveform	length	t_{step} (ns)	n_{step}(kHz)	ν_{max}(MHz)	a.a. filter	digitizer noise (nV/Hz$^{1/2}$)	
high freq.	10 μs	1	100	500	400 MHz	analog 5	digital 0.4/mV
standard	100μs	10	10	50	20 MHz	5	1.3/mV
low freq.	1 ms	100	1	5	20 MHz	5	4/mV

A standard run contains one thousand triggers. Each trigger yields two waveforms, one for each gain.

4.4 Spectrum analysis

A FFT of a subset of 2^n samples (up to 8192) is performed on both high and low gain waveform. The spectral analysis of 1000 triggers yields:

- two "single channel" analysis, i.e. the averaged spectra of the power and the phase
- a "coupled channel" analysis, i.e. the averaged spectrum of the complex correlation .

The power spectrum of the digitizer alone is subtracted from the overall power spectrum. Our digitizer, the DSA 602 from Tektronix, is equipped with a 20 and a 400 MHz anti-aliasing (a.a.) filters. This is sufficient to suppress aliasing noise, except for the low frequency sampling.

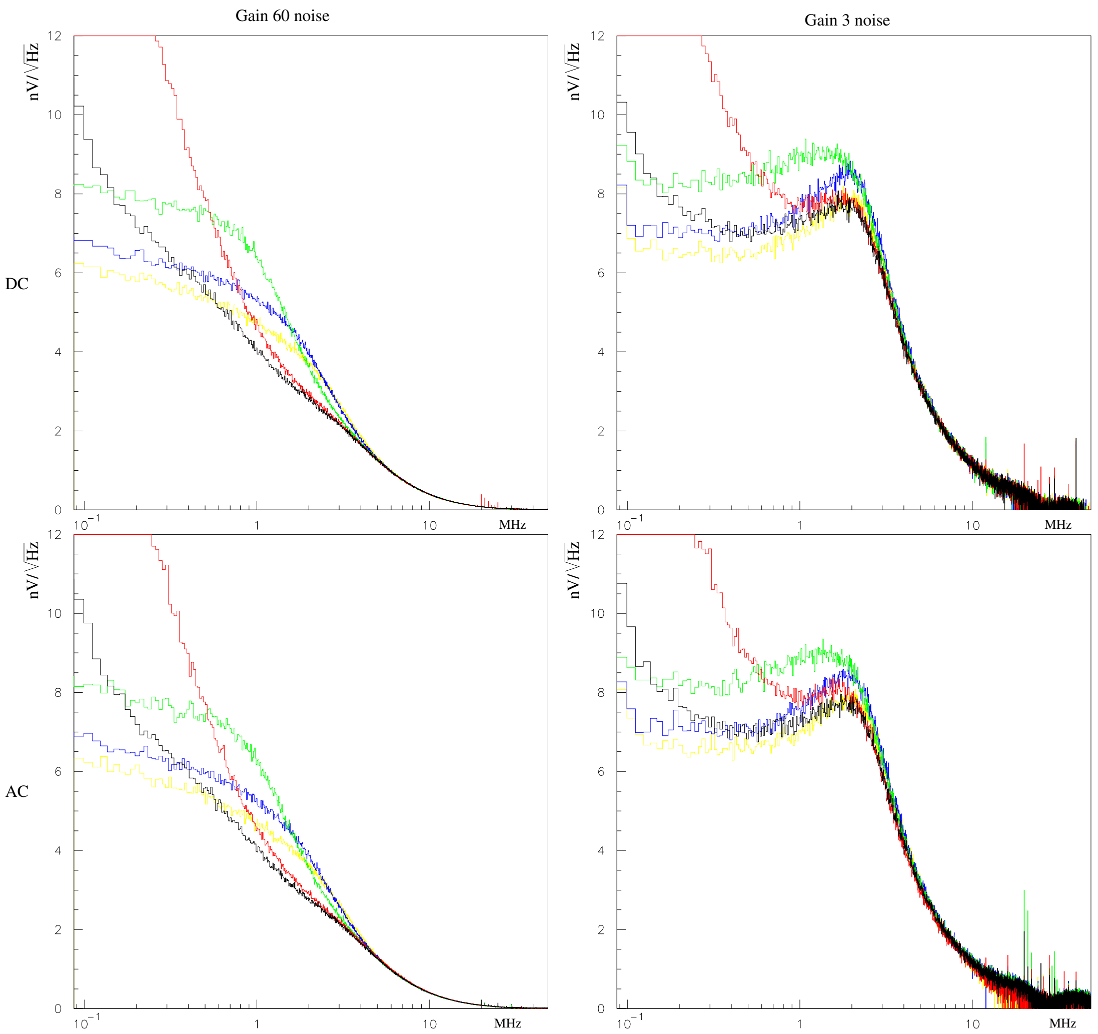

Figure 9: *Noise power spectra of the DGCS ASIC for 5 values of R_{CCD}: 50 (yellow), 500 (blue), 2k (green), 20k (red), 1MΩ (black). Top: DC mode / Bottom: AC mode - Left: gain x60 / Right: gain x3. Bare DSA spectra are subtracted. Output voltages are always divided by the gain.*

The coupled channel analysis is based on the statistical analysis of the complex covariance between the Fourier coefficients a_ν and b_ν of both high gain and low output signals at the same frequency ν. The covariance is the average on a set of many waveforms expressed by $C_\nu = < a_\nu \cdot \bar{b}_\nu >$, where $< a_\nu >$ and $< b_\nu >$ are null. The complex covariance C_ν can be transformed into a complex correlation $c_\nu = C_\nu/(s(a_\nu) \cdot s(b_\nu))$. Note that $s(a_\nu)$ and $s(b_\nu)$ are the noise power spectra shown in Figure 9. We represent in Figure 10 the correlation c_ν by its real and imaginary parts.

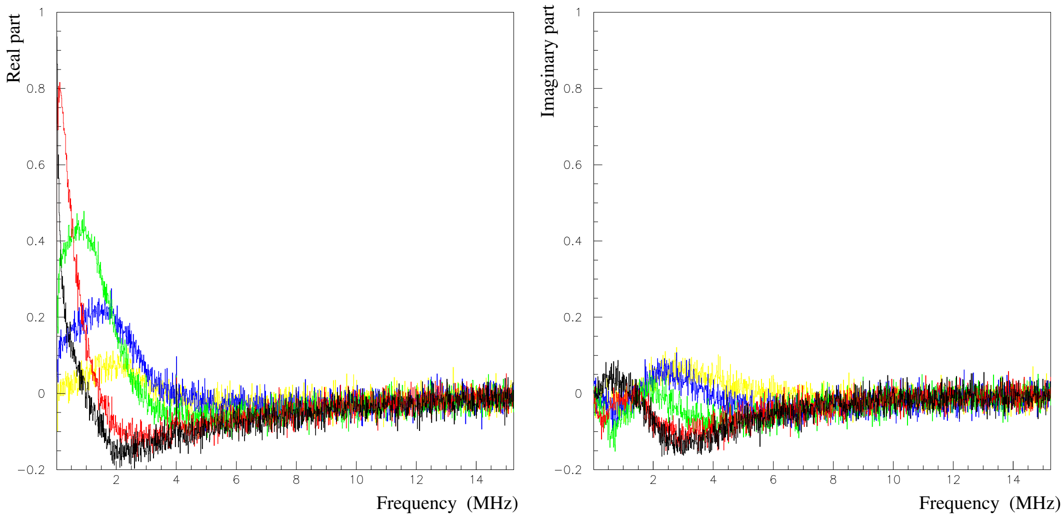

Figure 10: *Frequency spectra of the real and imaginary parts of the complex correlation coefficient of gain x3 and gain x60 amplifiers. They discriminate between "CCD noise" generated by the R_{CCD} at low frequencies, which is coherent, and amplifier noise, which is not.*

4.5 Digitization

The digitization depends on the vertical scale of our Tektronix DSA 602. The best sensibility is achieved with a 1 mV vertical unit (cf. rightmost column of Table 1), when our amplifier output signal can be mapped in a 10 mV window. In this case the digitizer noise, which have to be divided by the amplifier gain to be compared to the amplifier input noise, is small inside the band pass of the amplifier (around 2 $nV/\sqrt{Hz}$ for gain x3). Furthermore, for each set of waveforms "digitizer- with-amplifier", we measure the corresponding set of waveforms "digitizer- without-amplifier". The final spectra shown here are obtained by subtraction of spectra with and without amplifier. This procedure was shown to be unbiased up to 10-30 MHz. It allows us to measure the high frequency cutoff of our amplifier, from 6 down to 0.1 $nV/\sqrt{Hz}$.

4.6 Pickup noise

4.6.1 Pickup control

We have defined a severe set of requirements for noise measurements (an absolute precision of 1 μV (RMS) and a relative precision of 0.1 μV). In order to meet these requirements we had to eliminate pickup noise. This process was controlled by the following means:

- Checking the absence of big pickup "lines" in power spectra (Figure 9)
- Separating the amplifier noise spectra and the input resistor thermal spectra by varying R_{in} (kTR_{in} provides an absolute noise calibration, see section 6.1.1)
- Testing the noise corner estimators obtained by summing the amplifier output signal during 80 μs. As they are characterized by a small RMS dispersion $\sigma_{input} \approx 1.2\,\mu$V, a pickup, let say 0.3 μV, would show up as an instability or a non-gaussian distribution. (Figure 11a)
- Computing the 'mean amplifier noise' (average of both gains) as a combination of 4 different variable waveforms, which cancels the common noise produced by R_{CCD} (cf Figure 11b). It indicates that the precision of our noise measurement is compatible with our 0.1 μV goal.

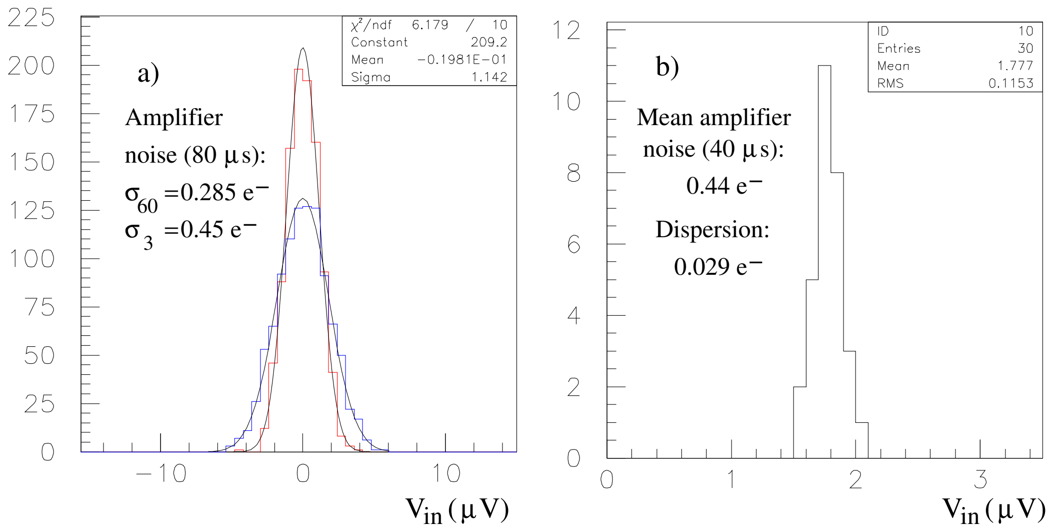

Figure 11: *a) Pedestal distribution for x60 and x3 amplifiers (with $R_{CCD} = 0$ and integration time $T = 80\,\mu s$), yielding the amplifier input noise estimates: $\sigma_{60} \simeq 1.14\,\mu V$ and $\sigma_3 \simeq 1.8\,\mu V$. b) The "mean amplifier noise" distribution is peaked around 1.77 μV with a dispersion of 0.1 μV (RMS) when the range of input components vary from $R_{CCD} = 0$ to $20\,k\Omega$ and from $C_l = 0.5$ to $2\,\mu F$ ($T = 40\,\mu s$).*

4.6.2 Pickup problems

Two pickup problems asked for some special attention:

1. Ground currents induced by the AC power supply.
   Our clamp and sample design needs a very good common ground between the CCD output section, the clamp input section and the ADC input. In our case our huge DSA digitizer cannot be put in a box with our ASIC. We had to optimize the grounding scheme in order to bring the 150 Hz noise down to a few μV, and then to use a line synchronous DSA trigger to push it down to a negligible level.

2. Parasitic coupling induced by the sweeping of the DSA screen.
   Its yields a 35 μV (< 1 LSB) parasitic signal at $30 \mu s$ period. Its effect was eliminated using a synchronous trigger and a software subtraction of the averaged parasitic signal (cf. Figure 12).

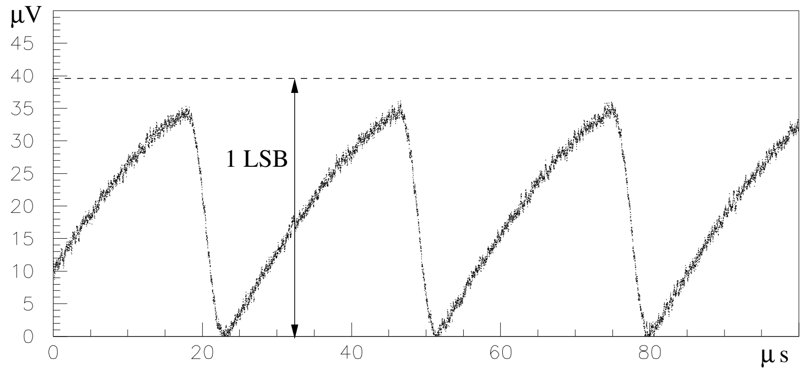

Figure 12: *Parasitic signal induced by the DSA digitizer, averaged over 1000 waveforms using a pickup-synchronous trigger (gain x3 amplifier input).*

The next generation of ASIC will integrate the ADC and the DGCS amplifier at the back of the CCD detector. This is a natural solution to suppress these pickup problems.

5 Simulation method

The basic design of DGCS ASIC has been simulated independently for each amplifier (gain x3 and x60). This approach yielded a noise simulation in good qualitative agreement with our experimental results.

The next step has been to simulate jointly both amplifiers within the test configuration of Figure 8 and to make the input resistance R_{CCD} vary, in order to reproduce the experimental results shown in the next section. Two simulations were needed:

- The introduction of the parasitic capacitances inside the ASIC are allowed by the AMS 0.35μ simulation kit. This is necessary to simulate second order effects such as the modification of the frequency cutoff of the amplifier and the coupling of both amplifiers through the input circuit. It is also needed to simulate a large bump around 2 MHz in the transfer function of the amplifier which is connected to the output of the multiplexer (cf. Figure 13).

- The introduction of parasitic impedances is incompatible with the parasitic capacitances. This limitation of our design kit prevent us to perform a global quantitative simulation to reproduce the design problems of our ASIC (a lower "high gain", a parasitic offset and an increased input resistance R_{CCD}, with a predictable effect on the input noise).

Finally we had to run each type of simulation independently in order to compare quantitatively the relative effect of each feature with the experiment. We found a good agreement in both approaches. This leads us to think that a simulation kit supporting both parasitic effects could be tuned to reproduce the experimental data within $\approx 5\%$. For the next ASIC to be designed it is hoped that parasitic resistances will be negligible, i.e. that the simulation with parasitic capacitances will be quantitatively correct.

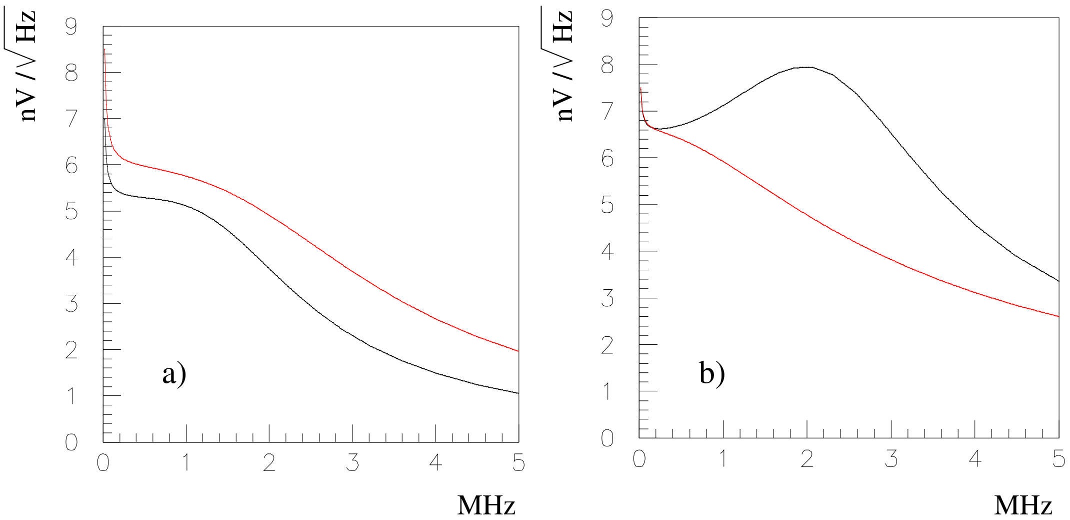

Figure 13: *Simulation of noise spectra, a) gain x60, b) gain x3. Black curves are for parasitic capacitances on and resistances off; red curves for parasitic capacitances off and resistances on (the simulator does not allow both at the same time). In this configuration gain x3 is connected to multiplexer output, causing the bump in b) due to parasitic capacitances.*

6 Results of experience and simulation at room temperature

Our analysis is based on two simple models of CCD readout: one for "double sampling" and one for a "clamp and sample". The former has two independent noise sources:

- the CCD noise produced in our setup by R_{CCD}, which is seen coherently by both amplifier channels,
- the amplifier noise seen incoherently.

For the clamp and sample model we add a "clamping noise" produced "instantly" at the unclamping moment (we shall see that this is not only the classical kTC noise)

- the clamping noise is seen coherently by both amplifier channels, but it is not independent of R_{CCD} noise, as we shall see.

6.1 Spectral analysis of amplifier and R_{CCD} noise

A reasonable model for the merging of R_{CCD} noise and amplifier noise is shown on Figure 14 .

$$\gamma_{out}(\nu) = \gamma_R(\nu) \cdot |G(\nu)|^2 + \gamma_{3,60}(\nu) + \epsilon(\gamma_R(\nu) \cdot |G(\nu)|^2 + \gamma_{60,3}(\nu)) \tag{1}$$

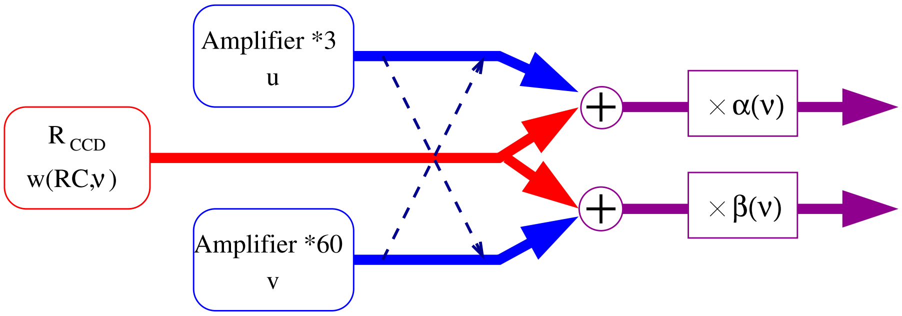

Figure 14: *Model of noise generation in ASIC.*

A small contribution of cross talk between gain x3 and gain x60 noise generators is shown by the cross channel analysis. It is not possible yet to reproduce it in the simulation due to technical limitations.

The analysis of measured and simulated noise spectra allows us to answer several pending questions:

Equivalence of DC and AC input configuration: For frequencies above 100 kHz there is no measurable difference between the noise spectra in the AC and DC input configurations, as seen in Figure 9 when comparing the upper and lower spectra.

Multiplexer enhancement: Agreement between experiment and simulation with parasitic capacitances. It is clearly due to cross talk induced by these capacitances in the output section of the ASIC (Figure 13).

Amplifier noise cutoff: Two different cutoffs are clearly distinguished when varying R_{CCD}: the R_{CCD} cutoff due to the input capacitance C_{in} of our setup, and the amplifier cutoff due to the bandwidth limitation of our ASIC design plus a contribution of parasitic capacitances seen in Figure 13.

Noise enhancement: The 15% noise enhancement shown by the simulation of parasitic resistances brings the total noise simulated near to the observed level of $\approx 6nV/\sqrt{Hz}$. However the design errors might contribute more than that.

6.1.1 R_{CCD} noise spectrum

Our goal here is to extract the thermal noise spectrum of the input resistor (R_{CCD}), to check its compatibility with thermodynamics, and to identify the capacitor shaping it. The data comes from a set of low frequency runs (1 ms in total) without any clamping or link capacitor.

With a model for the output noise spectrum without coupling between amplifiers:

$$\gamma(\nu) = \gamma_R(\nu) \cdot |G(\nu)|^2 + \gamma_{amp}(\nu) \tag{2}$$

The subtraction of two noise power spectra with input resistors R_1 and R_2 respectively ($\gamma_1(\nu)$ and $\gamma_2(\nu)$) eliminates the amplifier noise and yields:

$$\frac{\gamma_1(\nu) - \gamma_2(\nu)}{|G(0)|^2} = (\gamma_{R1}(\nu) - \gamma_{R2}(\nu)) \cdot \frac{|G(\nu)|^2}{|G(0)|^2} \tag{3}$$

According to thermodynamics, the thermal noise power spectrum of a resistor R, cut by a capacitor C, follows a Breit-Wigner or Lorentzian equation:

$$\gamma_R(\nu) = \frac{4\,k_B\,T\,R}{1 + (\frac{\nu}{\nu_c})^2} \qquad \text{with:} \qquad \nu_c = \frac{1}{2\pi\,R\,C} \tag{4}$$

This gives the two well-known quantities:

$$\gamma_R(0) = 4\,k_B\,T\,R \qquad \text{and:} \qquad \sigma_R^2 = \int_0^\infty \gamma_R(\nu)\,d\nu = \frac{k_B\,T}{C}$$

To obtain the power spectra of the input resistors, we subtract the lowest resistor power spectrum (50Ω) from the others. There are two major conditions for this operation to be successful:

- The difference in resistor values should be at least an order of magnitude, and more for more precise measurements. This makes the lowest resistor spectrum equivalent to a negligible baseline on the frequency range where the highest resistor noise is significant.

- The amplifier frequency response $|G(\nu)|^2/|G(0)|^2$should stay close to 1 on the same range. The frequency cutoff (ν_c) of the resistor noise should be much lower than the amplifier cutoff.

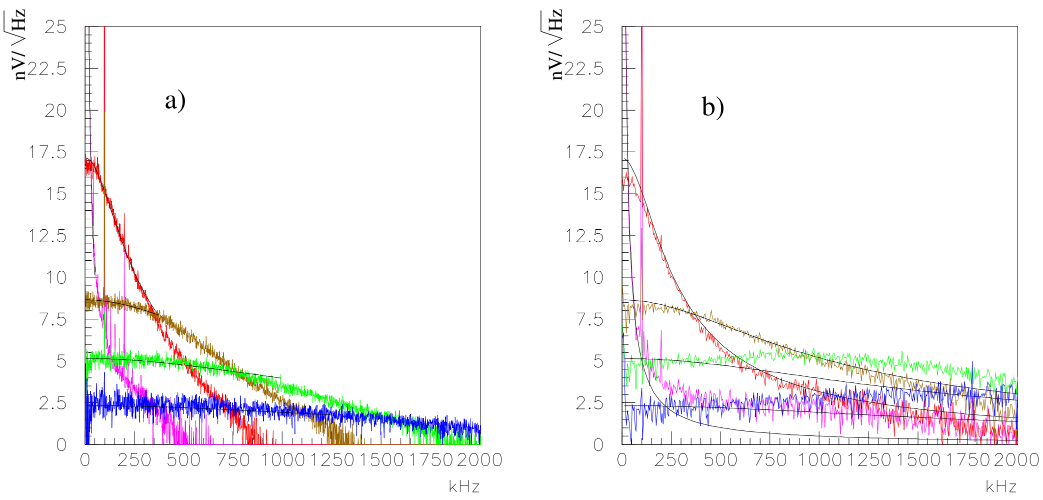

Figure 15: *a) Spectra for 5 values of R_{CCD} (gain x60 output): 500 (blue), 2k (green), 5k (brown), 20k (red), 1MΩ (magenta). Fits with Lorentzian function. b) Same spectra obtained from gain x3 outputs, superposed with the same functions as for gain x60.*

As a consequence, the fit is done in the lower frequencies, in most cases below cutoff, as can be seen Figure 15 (left). In the higher frequencies, the noise spectra of the others resistors plunge below that of $50\ \Omega$, and the subtractions deviate from the Lorentzian shape. As a test of the extraction method, the subtraction was applied to gain x3 outputs from the same runs, and the resulting spectra were compared with the fits obtained with the high gain data. The values at maximum are well matched, and so are the fits. However, above 500 kHz, most spectra show a 'bump', probably because the subtraction does not eliminate crosstalk noise properly.

Table 2 shows the parameters of the fitted curve for each input resistor, along with the temperature deduced from the maximum and the capacitor value deduced from the cutoff of the fit. For the lower resistor values, the later is too high, partly because of the access resistor value on the input (roughly taken into account in the last column), partly because of the cutoff of the amplifier.

R_{CCD} (Ω)		$4kTR_{CCD}$ (nV^2/Hz)	ν_c (kHz)	T (K)	C_+ (pF)
'1M'	1M	17330 ± 130	3.85 ± 0.02	314	41.4
'20k'	20.0k	294 ± 2	188 ± 2	267	41.3
'5k'	5.09k	74.9 ± 0.8	750 ± 40	269	38.0
'2k'	1820	26.5 ± 0.3	1210 ± 50	271	56.7
'500'	465	5.42 ± 0.13	1500 ± 100	237	110

Table 2: *Results of Breit-Wigner fits on R_{CCD} spectra obtained from subtraction. T is calculated from $4\,k\,T(R-50)$, C_+ (pF) from $\nu_c = 1/(2\pi\,(R+r_+)\,C_+)$ with a $500\ \Omega$ additional access resistor (r_+). We obtain a reliable value for the parasitic input capacitor from the first values of C_+; for the lower R_{CCD}, it is biased by the amplifier cutoff.*

6.1.2 Evaluation of access resistor with R_{CCD} spectra crossovers

According to equation 2, if two spectra intersect at frequency ν_i:

$$\begin{aligned}
\gamma_1(\nu_i) &= \gamma_2(\nu_i) \\
\gamma_{R_1}(\nu_i) \cdot |G(\nu_i)|^2 + \gamma_{amp}(\nu_i) &= \gamma_{R_2}(\nu_i) \cdot |G(\nu_i)|^2 + \gamma_{amp}(\nu_i) \\
\gamma_{R_1}(\nu_i) &= \gamma_{R_2}(\nu_i)
\end{aligned}$$

With the thermal noise (equation 4):

$$\begin{aligned}
\frac{4\,k_B\,T\,R_1}{1+(\nu_i \cdot 2\pi\,R_1\,C)^2} &= \frac{4\,k_B\,T\,R_2}{1+(\nu_i \cdot 2\pi\,R_2\,C)^2} \\
\frac{1+(2\pi\,R_1\,C\,\nu_i)^2}{R_1} &= \frac{1+(2\pi\,R_2\,C\,\nu_i)^2}{R_2} \\
(2\pi\,C\,\nu_i)^2(R_1-R_2) &= \frac{1}{R_2} - \frac{1}{R_1} \\
\nu_i^2 &= \nu_1 \cdot \nu_2
\end{aligned}$$

In this model for the noise spectra, this relationship is independent of the amplifier response. However, the accuracy of the measure of ν_i decreases with the resistors values, in the same way that the accuracy of the Lorentzian fits did. Several reasons for this problem can be put forward:

- The shape of the frequency response of the amplifier: it smooths down the noise spectra at the higher frequencies. This affects directly the accuracy of each measure.
- Aliasing, since the Nyquist frequency is 5 MHz for these 10,000-points, 1 ms runs.

- Crosstalk between amplifiers. This could explain the wide disparities between the two gains for the low resistors.

If we introduce the access resistor r_+ on the '+' input of the amplifiers:

$$\nu_i^2 = \frac{1}{(2\pi C)^2 (R_1 + r_+) \cdot (R_2 + r_+)} \tag{5}$$

$$r_+ = \sqrt{\frac{(R_1 - R_2)^2}{4} + \frac{1}{(2\pi C \nu_i)^2}} - \frac{R_1 + R_2}{2} \tag{6}$$

$$\tag{7}$$

For the 20k-5k intersection, $\nu_i = 350 \pm 5$ kHz (for both gains). Taking $C = 41$ pF and the measured values of the resistors, we obtain $r_+ = 820 \pm 130\Omega$. This value is compatible with the access path in the actual chip layout.

6.1.3 1/f noise and noise corner

In order to measure 1/f noise contribution we made a spectral analysis with the low frequency time window of 1 ms (cf Table 1). The 1/f noise is seen for lower values of R_{CCD} below 40 kHz frequencies and equals white noise contribution around 10 kHz. As shown in Figure 16 spectral analysis and AMS 0.35μ simulation agree perfectly on this point. This result does not tell us practically where the noise corner is. (Practical noise corner is where the SNR of CCD readout is optimum when we vary the width of the impulse response of an integrating filter). Figure 17 shows that this corner is at $\approx 300\mu s$ for an ideal double sampling filter ($150\mu s$ for a simple sampling filter)

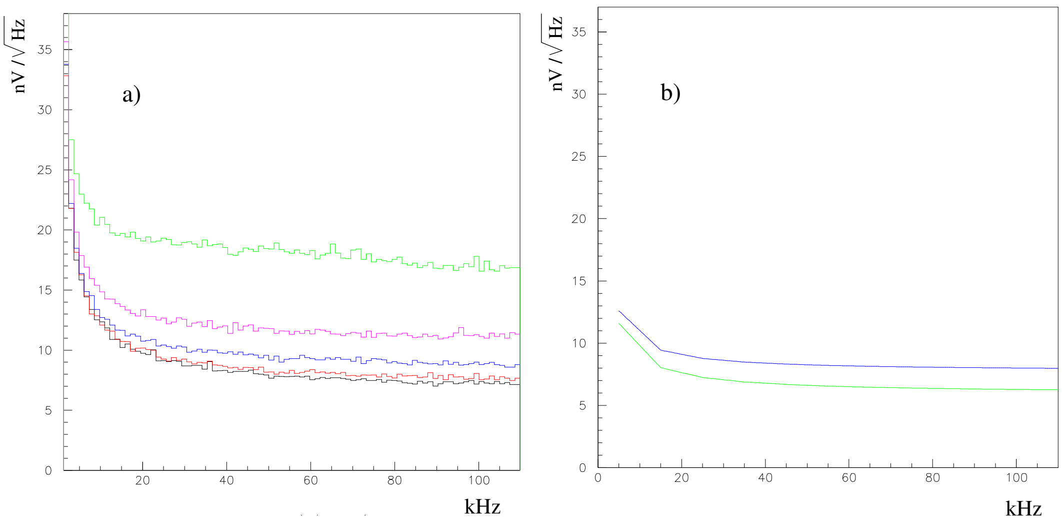

Figure 16: *1/f contribution: a) FFT spectra of gain x60 amplifier signal for 1 ms long waveforms (R_{CCD} varying from 0 to 20 $k\Omega$). b) AMS simulations for R_{CCD} of 0.5 and 2 $k\Omega$.*

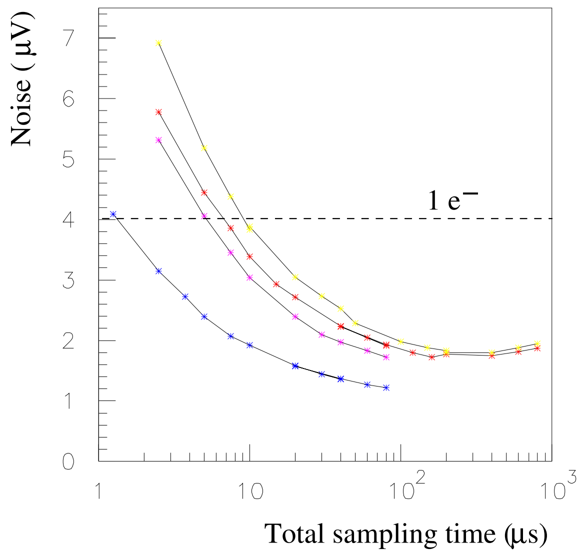

Figure 17: *Noise corner (the time scale is total time for one measure). From highest to lowest: correlated double sampling for 2000 and 500 Ω, with a contribution from aliasing; double sampling for 500 Ω without aliasing; 500 Ω with single sampling (and aliasing).*

6.2 Clamping noise

Our method for measuring the clamping noise consists in sampling twice the output of both amplifiers before and after a clamp period (in fact an infinite alternations of clamps and samples). The initial reason was to digitize both samples in a most similar way with the highest gain of the digitizer (rather than comparing two consecutive clamp and sample levels which differ by a few hundred millivolts). It turned out to be the very sensitive method needed to measure our clamping noises ranging from 1.3 to 3 μV. It was also applied to two clamps separated by a sample period in order to test the quality of clamping to a level small compared to the clamping noise itself.

Two other tricks are used in order to reach a maximal sensitivity:

- we measure each sample during $40\,\mu s$, as suggested by the noise corner curve (see Figure 9)
- we combine the measurements done independently by each amplifier channel.

Finally the results are in agreement with a kT/C_l formula as seen in Figure 18.

Let us note that this is not, strictly speaking, the kT/C switching noise of the clamp switch. This one is governed by the C_{in} parallel capacitance. We measured this effect independently by setting $R_{CCD} = \infty$. We found a much larger noise ($11\,\mu V$) in accordance with the measured value of $C_{in} = 40\,pF$.

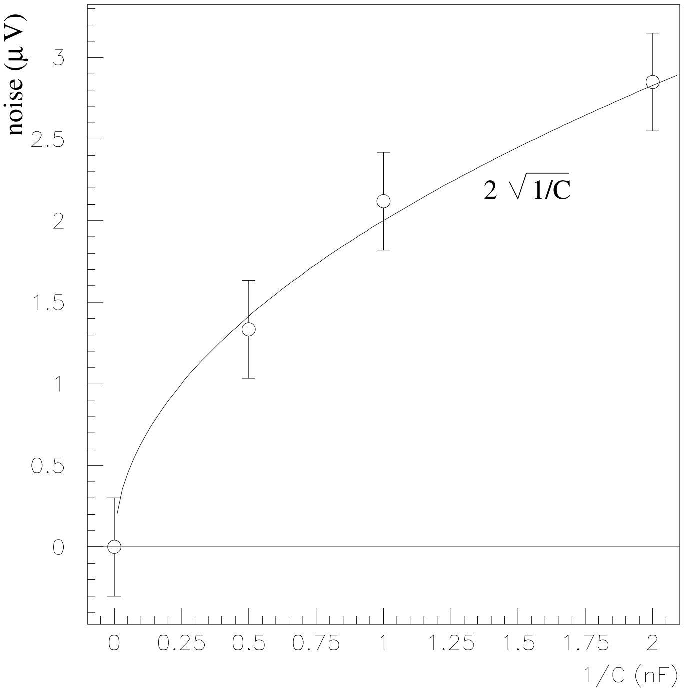

Figure 18: *Clamping noise as a function of C_l. The curve is the theoretical expression $\sqrt{kT/C_l}$ at $T = 290\,K$. The error bars are computed from the dispersion of switching noise when R_{CCD} vary from 0 to 20 $k\Omega$.*

7 Cold tests

The DGCS has been tested inside the cryostat developed for an IR pixel detector and its cold electronics, to be described in another report (see picture in Figure 19). The DGCS board was surrounded by a thermal screen, which temperature can be fixed from 85 K to the room temperature. The DGCS package is directly cooled by a thermal braid down to 130 K. Its temperature is measured and recorded together with its output waveforms.

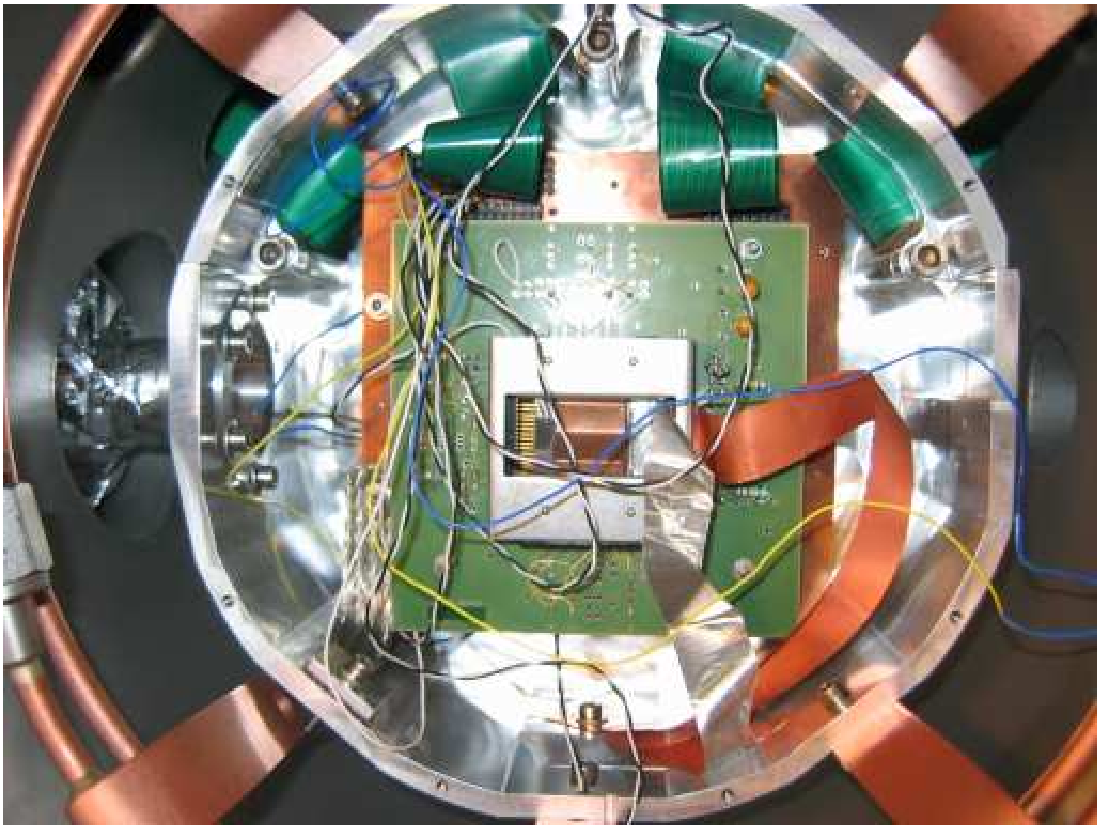

Figure 19: *Inner view of the IR bench cryostat showing the ASIC on its electronic card surrounded by the thermal screen.*

The main effect of cooling is to vary the offset and the gain of the high gain channel as seen in Figure 20. This is explained by the variation of parasitic resistances with temperature. It should vanish after fixing the corresponding design problem.

We have also studied the variation of DGCS noise spectra with temperature. Figure 21-a) show that the input noise of the x3 amplifier behave as expected for a thermal noise: it decreases roughly as $\sqrt{T}$ (see Figure 22 for a simulation). The x60 amplifier is more puzzling. There is a decrease of amplifier cutoff frequency and no change of input noise amplitude at low frequency. This behavior is hard to study since this channel is the one affected by parasitic resistors, which cannot be studied integrally by simulation. A simple explanation consists in accusing an extra noise source generated by parasitic resistors not proportional to gain. It would explain the noise difference between simulation and experiment. One might hope that it will disappear when correcting the ASIC layout, leaving a 20% smaller noise at T=290K, which would decrease with temperature in line with gain 3 channel.

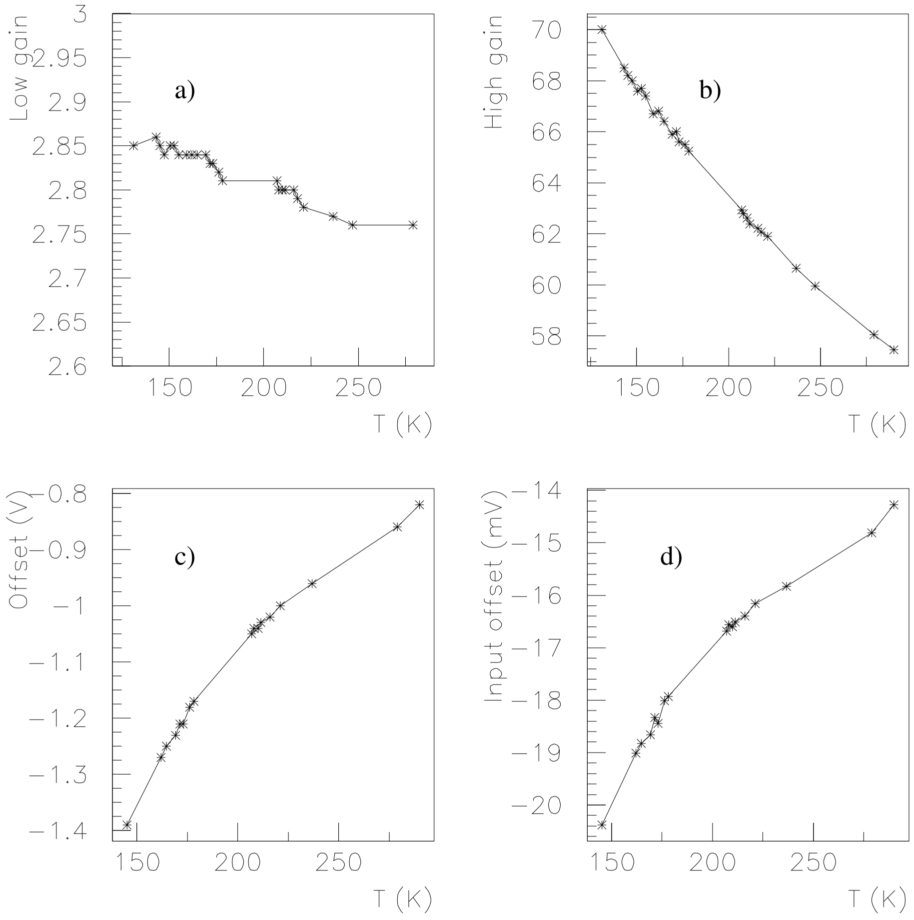

Figure 20: *Temperature sensitivity of gain and offset: a) low gain, b) high gain, c) high gain channel offset, d) same as c), divided by the gain.*

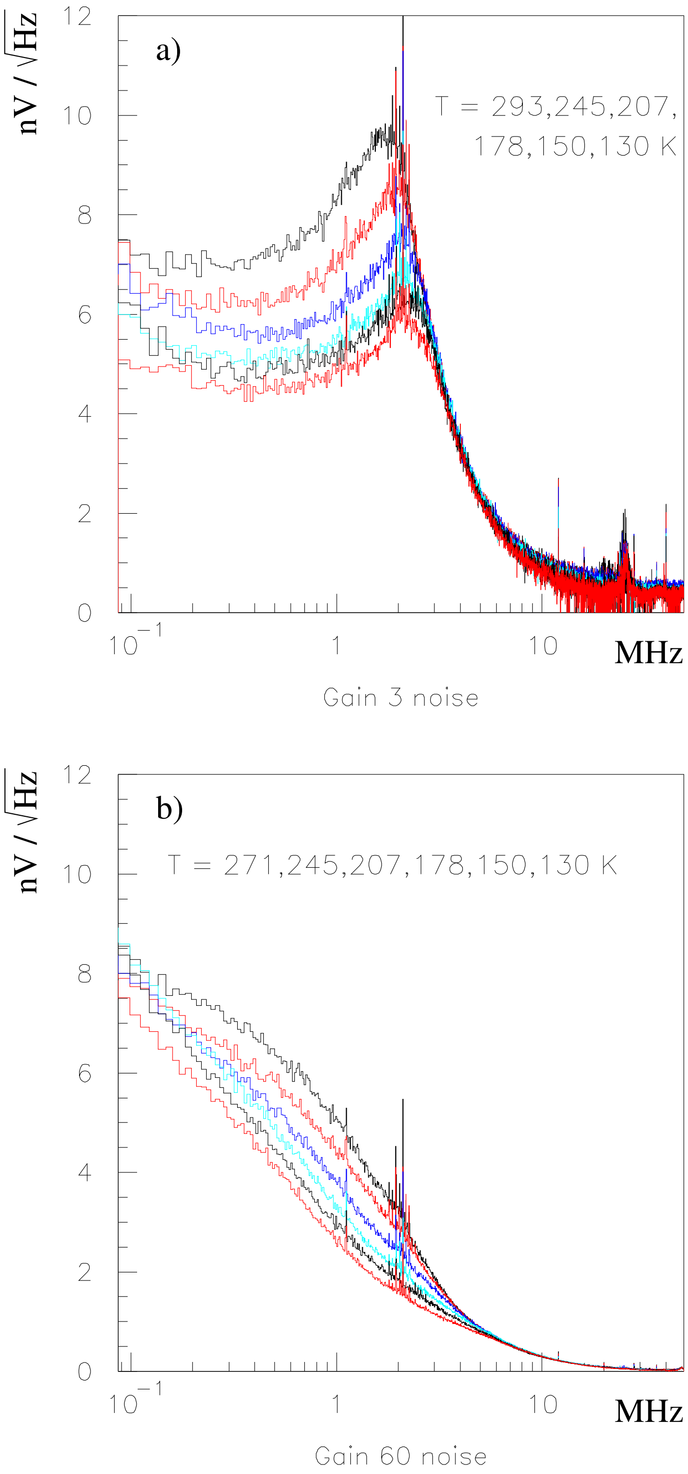

Figure 21: *Decrease of noise spectra with temperature . a) Low gain channel , b) high gain channel.*

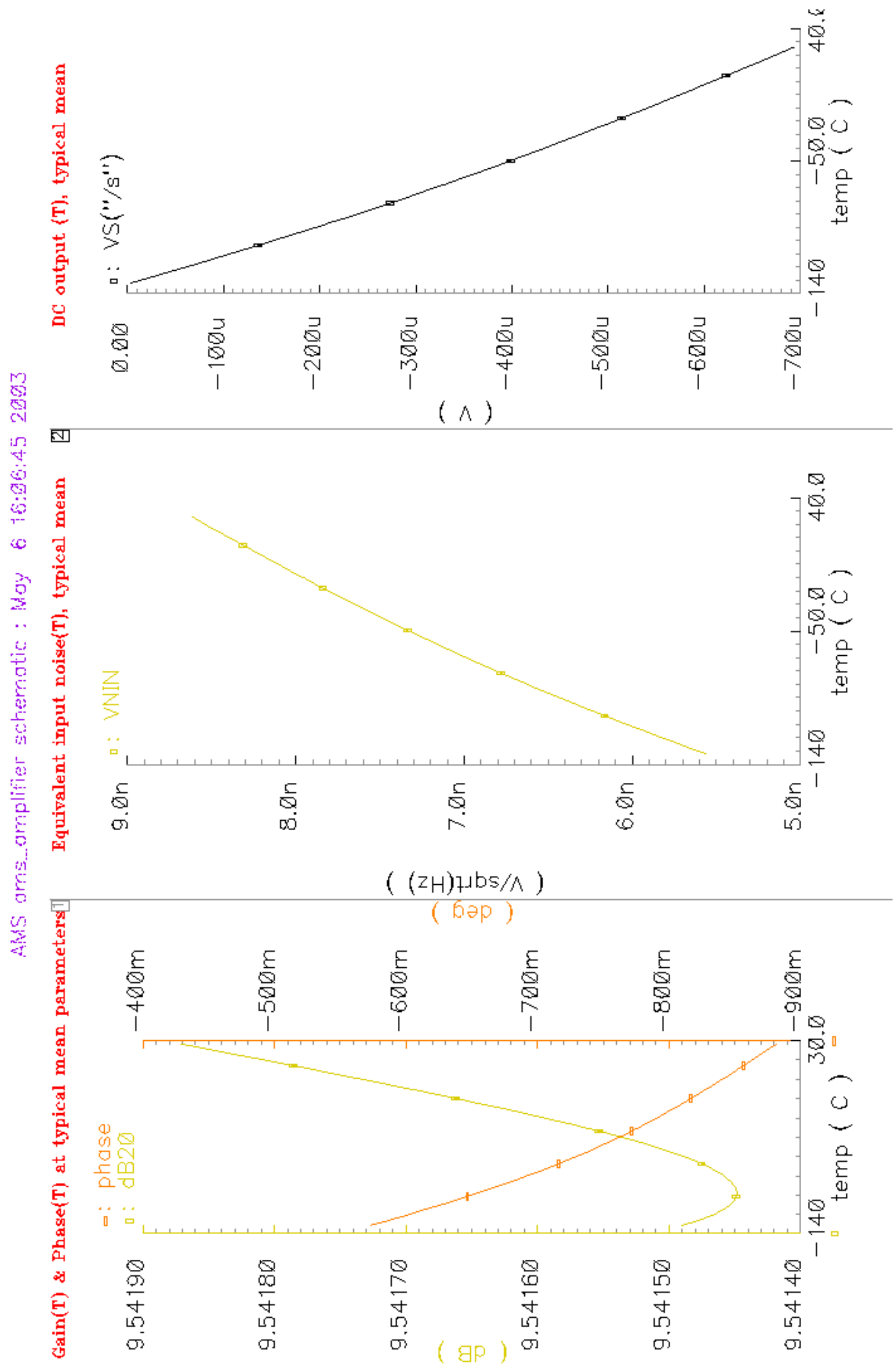

Figure 22: *Simulation of the x3 amplifier behavior as a function of temperature: gain and phase, noise, offset.*

8 Irradiation test

A DGCS ASIC has been irradiated with a 180 krad dose by a Cobalt 60 source at a rate of 1 krad per hour, after careful characterization of the test transistors present on this chip. The bondings of the chip were badly damaged during the process (not by radiation) and had to be remade. Afterwards, the same measures were made on the same test transistors. Some trends appear clearly (Figure 24): the transistors seem to be more or less sensitive to radiations depending on their dimensions; the effect is coherent for each separate type of transistors (NMOS and PMOS). However, it is still unclear how to account for all the effects.

To assess any effect on the overall functioning of the ASIC, both gains were measured as a function of frequency on the same setup for the irradiatied chip and another non-irradiated one (respectively red and black line on figure 23). We can see a slight increase in the high gain after irradiation. The offsets do not vary much either : from +12.2 mV to +11.6 mV for the low gain, and from -648 mV to -584 mV for the high gain.

To check whether this was indeed an effect of irradiation, the irradiated ASIC was heated at 100 °C for 50 minutes, which should reverse the effects of irradiation. Unfortunately, the NMOS transistors were destroyed during this process, but we still were able to do the measurements on the PMOS test transistors and on the two amplifier channels. The offsets are back to the values of a non-irradiated chip : +11.9 mV for the low gain offset, -650 mV for the high gain offset ; the same is true for the PMOS test transistor. However, graphics for the gains are more difficult to analyze, partly due to the fact that the non-irradiated chip could have a slightly different gain from the irradiated one from the start.

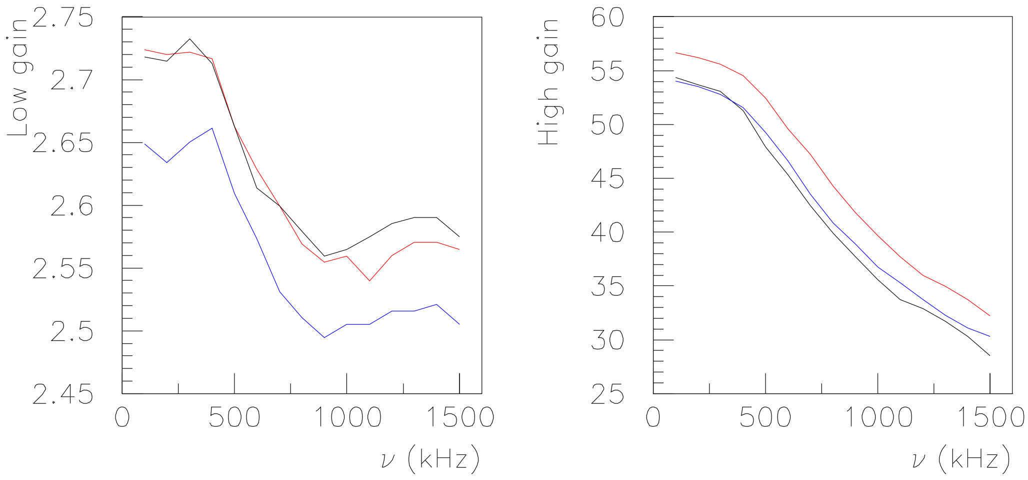

Figure 23: *Low and high gain measurements for a non-irradiated chip (black), the chip irradiated with a 180 kRad dosis (red), and the same after heating at 100°C for 50 minutes (blue).*

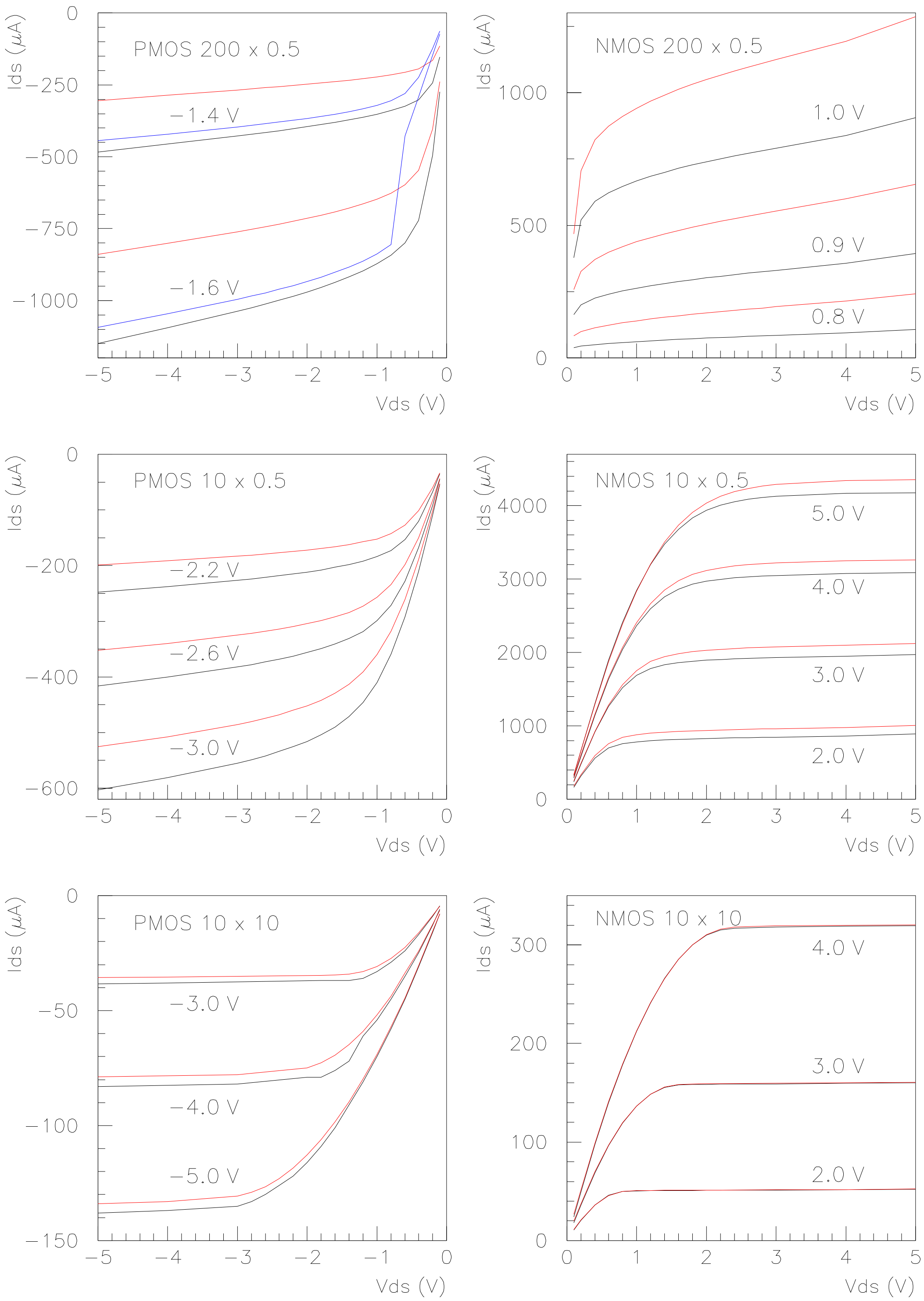

Figure 24: *Characteristics of each type of test transistors before (black) and after (red) 180 kRad irradiation, and after heating at 100°C for 50 minutes (blue).*

9 Conclusion

The dual gain clamp and sample (DGCS) function is a natural solution for a CCD readout circuit spanning a large dynamical range (17 bit SNR) with a sub-micron technology. A detailed electronic analysis of our DGCS ASIC, implemented using AMS-0.35μ process, has qualified it for SNAP noise, temperature and radiation requirements.

The method used for this analysis relies essentially on digital signal processing. It has allowed us to control external sources of noise down to 0.05 e- level. In addition, it has been able to evaluate and compare the effects of two filtering methods - either single sampling after clamping or correlated double sampling (CDS[5])-.

A particular attention was given to the former which will be implemented in the next step of our project. "Clamp and sample", compared to CDS, reach a given noise target either faster or with a simpler filtering scheme, at a cost of an extra sensitivity to low frequency noise. This extra sensitivity imposes either a compact electronics layout or, as in our setup, a rather tedious fight against pickup noise.

The optimization of the noise figure results of a choice of external components and of timing constants. In particular the contribution of clamping to the noise budget, which is of the order of half an electron, has been measured precisely as a function of the AC coupling capacitor, as well as the respective contributions of the CCD and the ASIC to the f^0 and f^{-1} overall noise.

The balance sheet of our DGCS ASIC looks as follows: a bandpass $\approx$3 MHz, matched to a 1 kΩ * 50pF CCD output, yielding a maximum data rate $\approx$1 Mpixel/s; a signal to noise ratio improving first as the inverse square root of the rate, then slower, down to around 0.5 e^- at 10 kpixel/s (corresponding to a noise corner at 300μs); a thermal noise density equal to 4.5 nV/$\sqrt{Hz}$ at 140 K making the cold ASIC comparable to the best CCD readout amplifiers at room temperature (these op-amp based amplifiers do not work at 140 K); power dissipation is 1.4 mW, small compared to a typical CCD.

The linearity of the dual gain amplifier has been analysed with a 20 bit resolution pulse generator. As a by-product we could confirm precisely our diagnostic for the non conformities of the ASIC due to parasitic resistors not accounted for in the AMS 0.35μ design kit. This <0.1% linearity is as usual too good to be true. In fact one should remember that the real non linearities are due essentialy to the transient response which is not well simulated with a pulse generator.

Therefore this series of electronic tests will be completed with another using our CCD test bench as a pulse generator.

[5] note that correlated double sampling should also begin with a clamping phase synchronized with CCD reset, because of the necessity to restore DC level at the amplifier input.

A Layout schematics of the DGCS amplifier

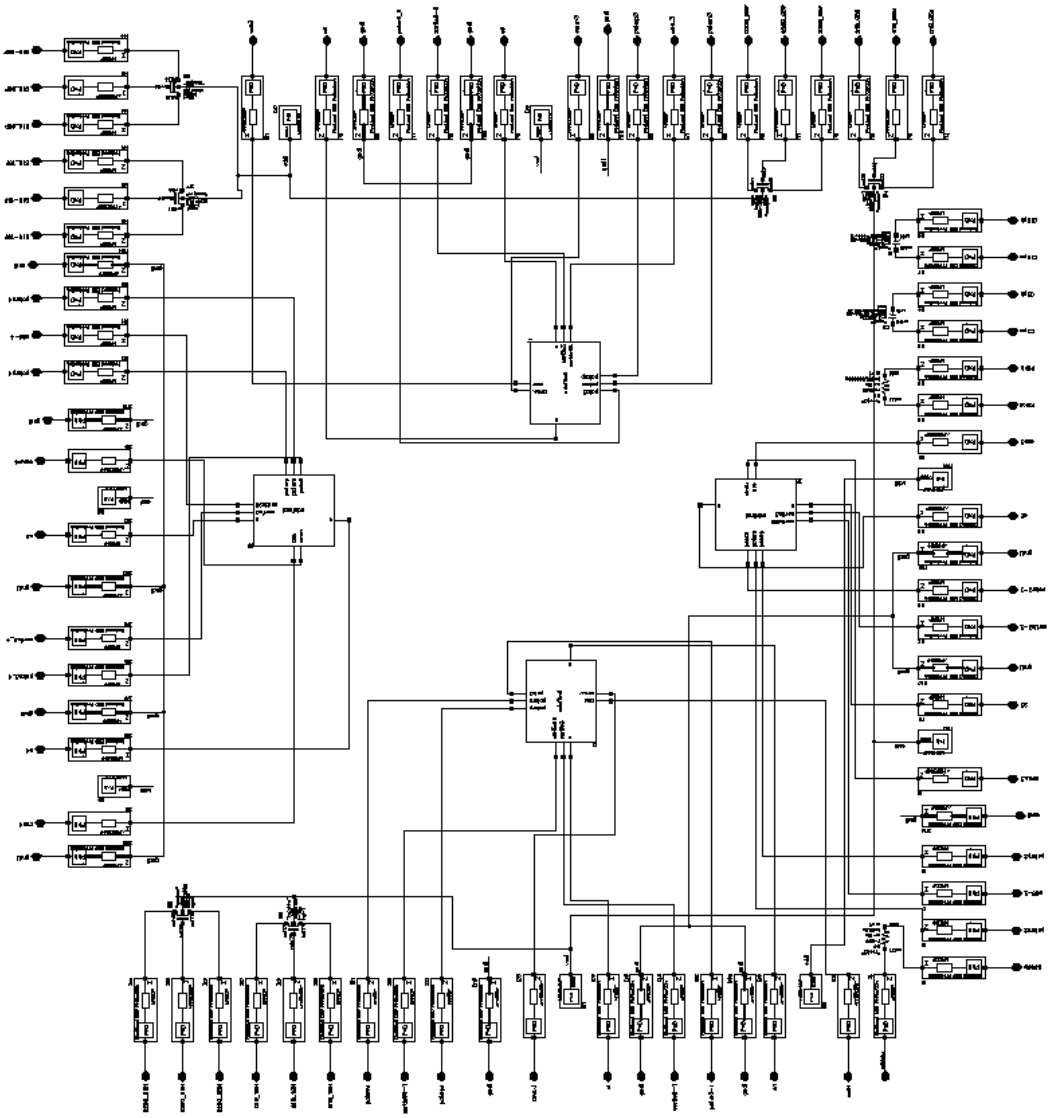

Figure 25: *Chip layout.*

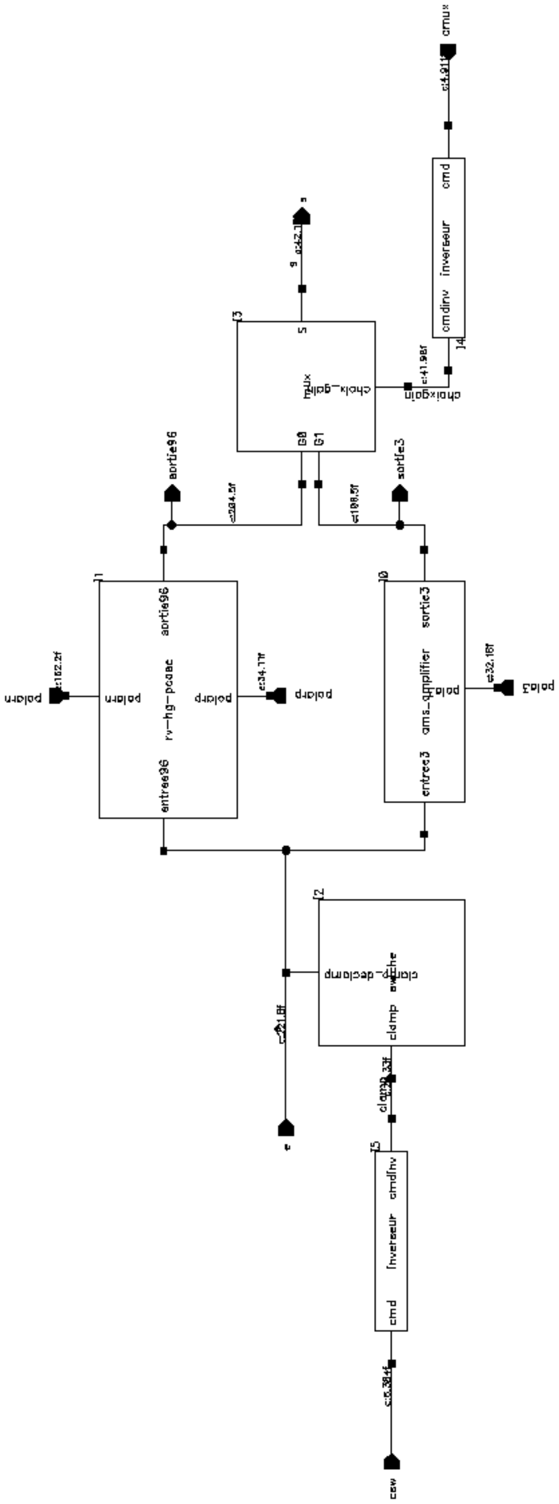

Figure 26: *Amplifier block diagram.*

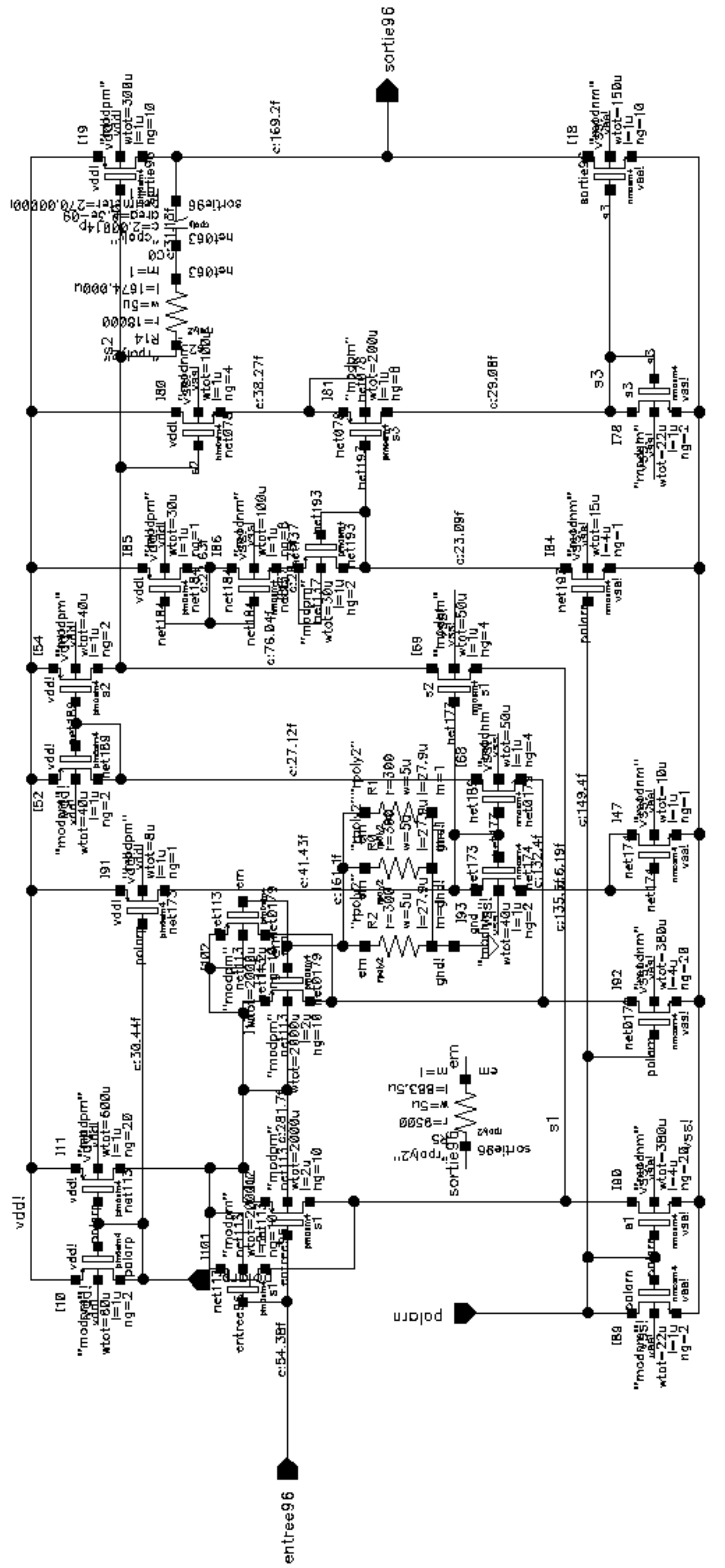

Figure 27: *High gain schematics.*

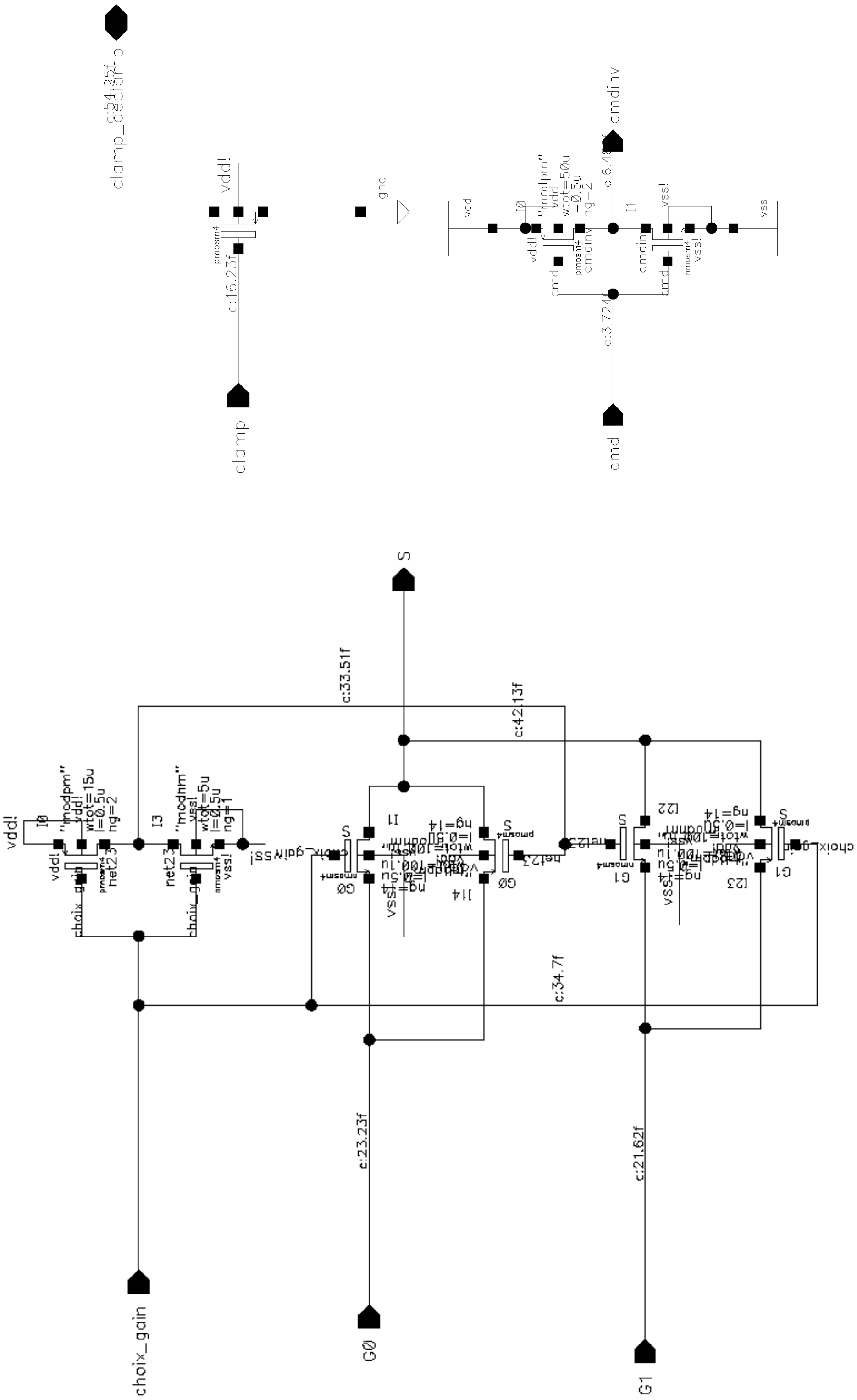

Figure 28: *Clamp, inverter and multiplexer.*

B Simulation of the high gain problems with parasitic resistors

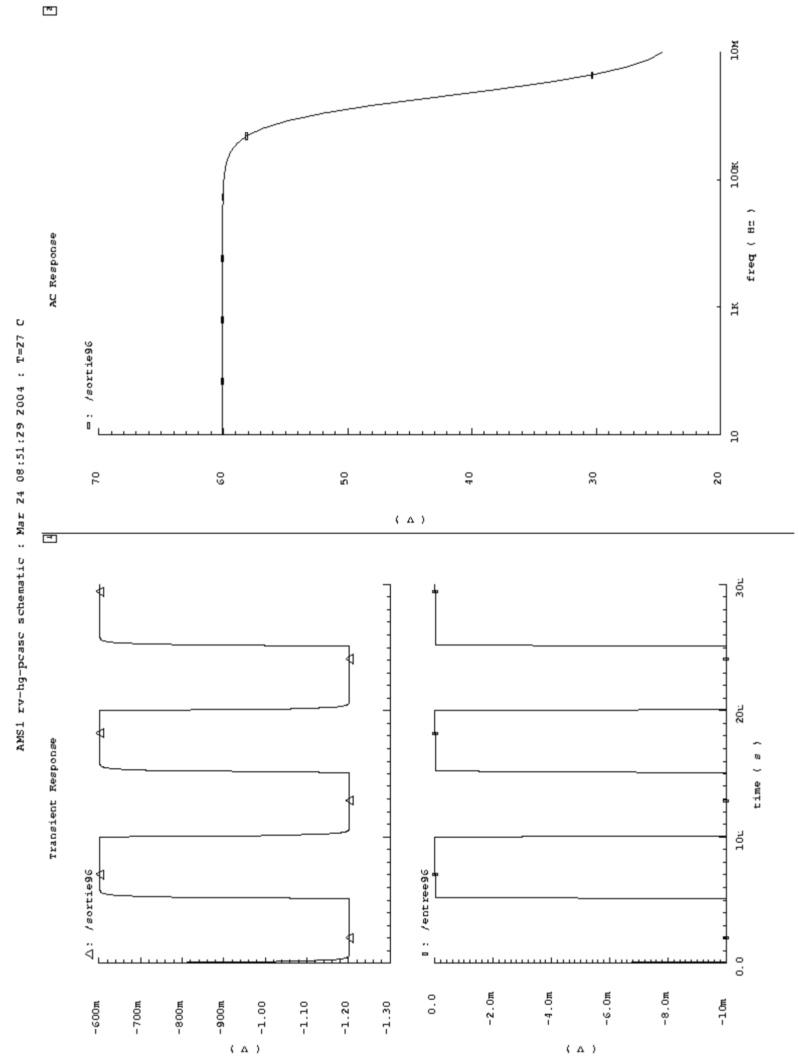

Figure 29: *High gain channel gain, offset and bandpass simulation with parasitic resistors.*